Ultra-Low Phase Noise LVPECL, LVDS Buffer & Translator

Description

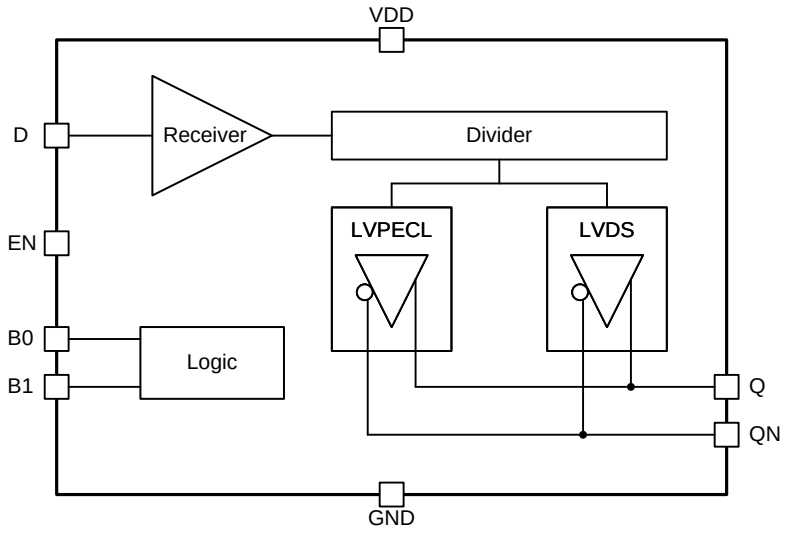
The AZS15 is a configurable LVPECL, LVDS buffer & translator IC that is optimized for ultra-low phase noise and additive jitter operating at 2.5V & 3.3V nominal supply voltages. It is particularly useful in converting crystal or SAW based oscillators into LVPECL and LVDS outputs for signals up to 1.5GHz. For designs with larger signal amplitude, consider the AZS10 which has more input receiver bandwidth.

The AZS15 is a configurable IC design capable of providing LVPECL or LVDS outputs, ÷1 or ÷2 function, and active high or active low enable selection. See Table 7 for details of the configurations options that provide designers with a single high performance IC buffer/translator solution that is extremely compact and flexible.

Features

- Ultra-low phase noise floor
  - LVPECL: -167dBc/Hz
  - LVDS: -165dBc/Hz
- Selectable LVPECL/LVDS output levels
- Internal divide by two
- Enable active high or low
- Output frequency up to 1.5GHz
- Up to 125C operation

Block Diagram



Applications

- Crystal or SAW based oscillators
- Sampling system clock driver
- LVPECL/LVDS clock reference and drivers
- LVPECL/LVDS signal conversion

Ordering Information

Order Number	Package	Reel Quantity	Marking	MSL Rating	Leadframe
AZS15QGR1	SON8	1000	R<date code>	1	NiPdAu
AZS15TGR1	MSOP8	1000	BE5G / <Date Code>	1	NiPdAu

Specifications

Table 1 Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage	±10%	2.97	3.3	3.63	V
	±5%	2.375	2.5	2.625	
Operating Temperature		-40	27	125	°C

Table 2 General Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input Bias Resistor	D Input to Vdd/2 Reference		10k		Ω
Input Voltage Swing		0.2			Vpp
		-10			dBm
Input High Voltage Threshold	EN, B0, B1	V_{DD} - 0.5		V_{DD}	V
Input Low Voltage Threshold	EN, B0, B1	0		0.5	

Table 3 LVPECL Output Specifications

Typical values applicable under the conditions of V_{DD} = 2.5V-3.3V, T_A = 27˚C, unless otherwise noted

Minimum and maximum values are given over full V_{DD} and T_A variation (-40˚C to + 125˚C), unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Input Frequency	÷ 1			1500	MHz
	÷ 2			1600	
Output Loading			50		Ω
DC Output Levels	V_{DD} = 3.3V, HIGH	V_{DD}-1.15		V_{DD}-0.88	V
	V_{DD} = 3.3V, LOW	V_{DD}-1.86		V_{DD}-1.75	V
	V_{DD} = 2.5V, HIGH	V_{DD}-1.25		V_{DD}-0.88	V
	V_{DD} = 2.5V, LOW	V_{DD}-1.86		V_{DD}-1.66	V
Differential Output Voltage	V_{DD} = 3.3V	0.74		0.93	V_{pp}
	V_{DD} = 2.5V	0.54		0.93	V_{pp}
Output Rise/Fall Time	80% - 20%	100		205	ps
Phase Noise Floor[1]	155MHz, 1MHz Offset	-167			dBc/Hz
Additive Jitter	155MHz carrier: 12kHz-20MHz		38		fs
Enable Time[2]				15	us
Disable Time[2]				0.5	us
Propagation Delay[3]		0.9		2.2	ns

1 Phase noise floor performance is dependent upon input voltage swing and slew rate. Voltage swing values below recommended values may result in degraded phase noise values.

2 Into and out of tri-state condition

3 Time from D crossing V_{DD}/2 to Q=QN

Table 4 LVDS Output Specifications

Typical values applicable under the conditions of V_{DD} = 2.5V-3.3V, T_A = 27˚C, unless otherwise noted

Minimum and maximum values are given over full V_{DD} and T_A variation (-40˚C to + 125˚C), unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Input Frequency	÷ 1			1500	MHz
	÷ 2			1600	
Output Loading			100		Ω
Voltage Output Levels	V_{DD} = 3.3V	290		454	
	V_{DD} = 2.5V	290		454	
Differential Output Voltage		-50		50	V
Common Mode Output Voltage		1.125		1.375	V
Delta in Common Mode Output		-50		50	mV
Peak-to-Peak Common Mode Output				100	mV
Output Rise/Fall Time	80% - 20%	120		220	ps
Phase Noise Floor[1]	155MHz, 1MHz Offset	-165			dBc/Hz
Additive Jitter	155MHz carrier: 12kHz-20MHz		70		fs
Enable Time[2]				4	us
Disable Time[2]				0.5	us
Propagation Delay[3]		0.8		1.7	ns

1 Phase noise floor performance is dependent upon input voltage swing and slew rate. Voltage swing values below recommended values may result in degraded phase noise values.

2 Into and out of tri-state condition

3 Time from D crossing $V_{DD}/2$ to Q=QN

Table 5 Absolute Maximum Ratings

Parameter	Conditions	Min	Max	Unit
Supply Voltage		-0.5	V_{DD} + 0.5	V
Input Voltage		-0.5	V_{DD} + 0.5	V
Output Voltage		-0.5	V_{DD} + 0.5	V
Soldering Temperature			260	˚C
Storage Temperature		-55	150	˚C
Junction Temperature			150	˚C
ESD Ratings	Human Body Model	2000		V
	Machine Model	100		
	Charged Device Model	1000		

Pin Configuration and Functionality

Table 6 Pinout List

Pin	Name	I/O/P	Description	Properties
1	EN	I	Enable	Configurable functionality
2	Q	O	Output Signal	Configurable (LVPECL, LVDS)
3	QN	O	Output Signal	Configurable (LVPECL, LVDS)
4	GND	P	Negative Supply	0V
5	D	I	Input Signal	
6	B0	I	Configuration Bit	Tertiary Levels
7	B1	I	Configuration Bit	Tertiary Levels
8	VDD	P	Positive Supply	2.375V - 3.6V

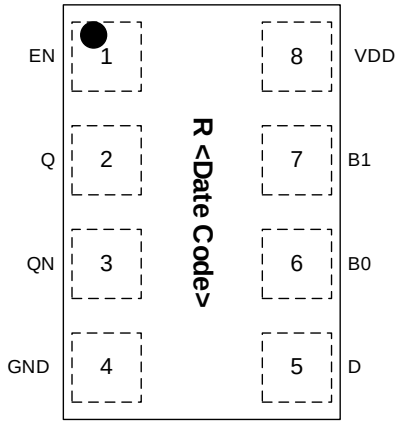


Figure 1 SON8 Package Pinout

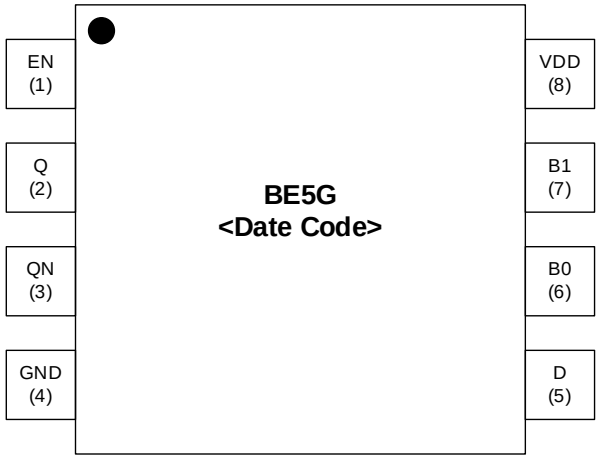


Figure 2 MSOP8 Package Pinout

The AZS15 has 8 configurations which are determined by the static voltage levels of B0 and B1.

Table 7 Functional Configurations

Configuration Bits		Functional Configuration		
B0	**B1**	**Output Type**	**Enable Polarity**	**Output Division**
Open	Open	LVPECL	Active High	÷1
Open	Low	LVPECL	Active High	÷2
Open	High	LVPECL	Active Low	÷1
Low	Open	LVPECL	Active Low	÷2
Low	Low	LVDS	Active High	÷1
Low	High	LVDS	Active High	÷2
High	Open	LVDS	Active Low	÷1
High	Low	LVDS	Active Low	÷2
High	High	not used	not used	not used

Application Notes

Input Termination

The D input bias is $V_{DD}/2$ fed through an internal 10kΩ resistor. For clock applications, an input signal of at least 750mV_{pp} ensures the AZS15 meets AC specifications. The input should also be AC coupled to maintain a 50% duty cycle on the outputs. The input can be driven to any voltage between 0V and V_{DD} without damage or waveform degradation.

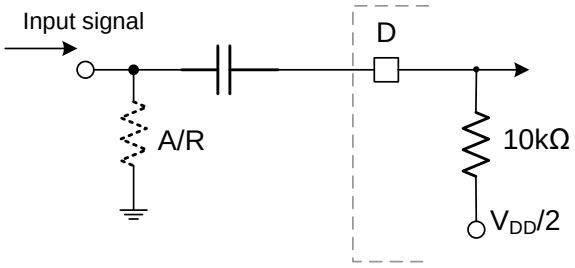


Figure 3 Input Termination

LVPECL Output Termination Techniques

DC Coupling

The LVPECL compatible output stage of the AZS10 uses a current drive topology to maximize switching speed as illustrated below in Figure 4. Two current source PMOS transistors (M1-M2) feed the output pins. M5 is an NMOS current source which is switched by M3 and M4. When M4 is on, M5 takes current from M2. This produces an output current of 5.1mA (low output state). M3 is off, and the entire 21.1mA flows through the output pin. The associated output voltage swings match LVPECL levels when external 50Ω resistors terminate the outputs.

Both Q and QN should always be terminated identically to avoid waveform distortion and circulating current caused by unsymmetrical loads. This rule should be followed even if only one output is in use.

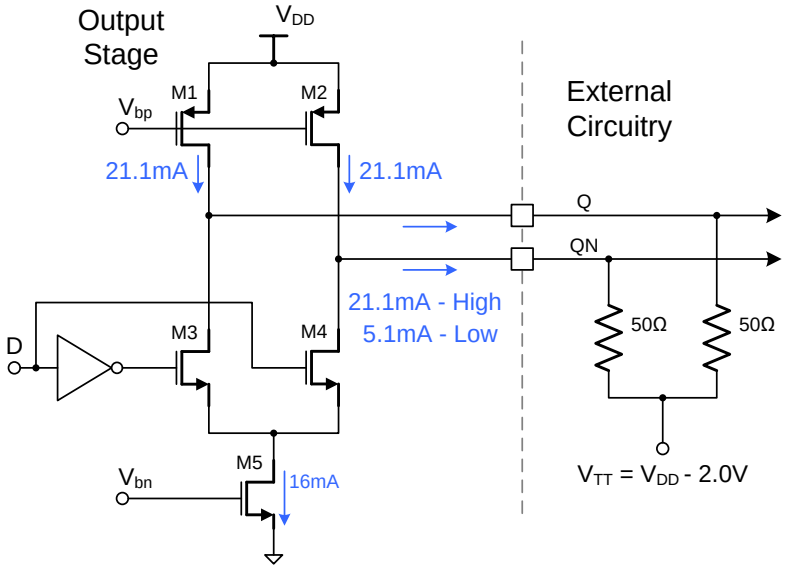


Figure 4 Typical Output Termination

AC Coupling

Clock applications or phase noise/frequency domain testing scenarios typically require AC coupling. Figure 5 below shows the AC coupling technique. The 200Ω resistors form the required DC loads, and the 50Ω resistors provide the AC termination. The parallel combination of the 200Ω and 50Ω resistors results in a net 40Ω AC load termination. In many cases this will work well. If necessary, the 50Ω resistors can be increased to about 56Ω. Alternately, bias tees combined with current setting resistors will eliminate the lowered AC load impedance. The 50Ω resistors are typically connected to ground but can be connected to the bias level needed by the succeeding stage.

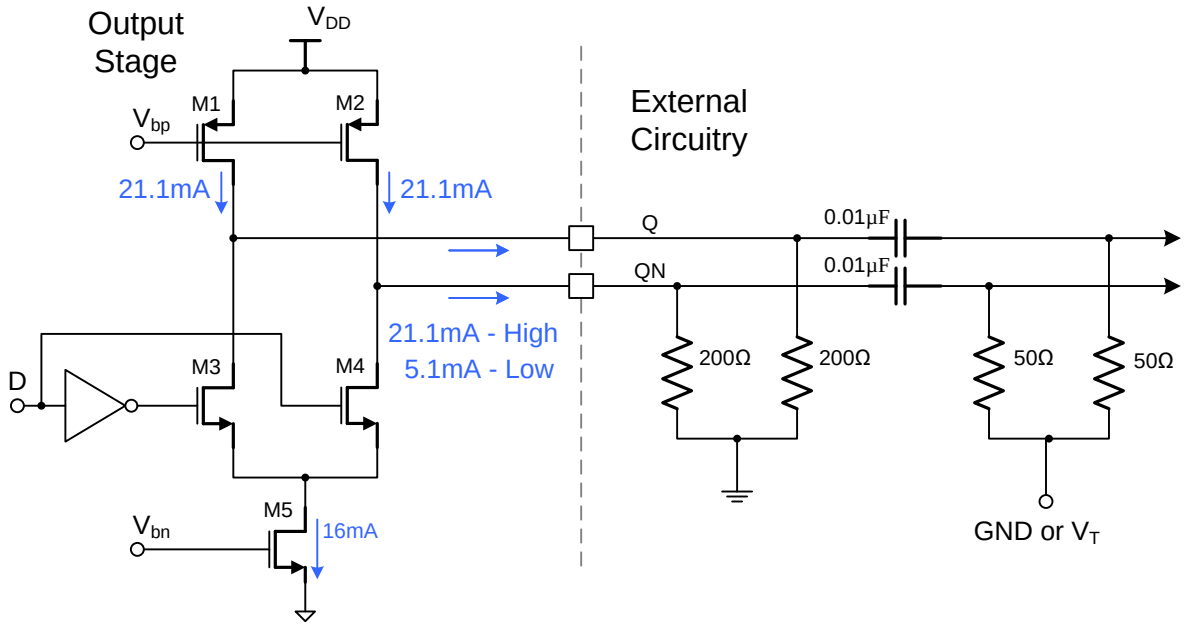


Figure 5 AC Termination

LVDS Output Termination Technique

The following LVDS termination is compliant to the LVDS specification *TIA/EIA-644A*.

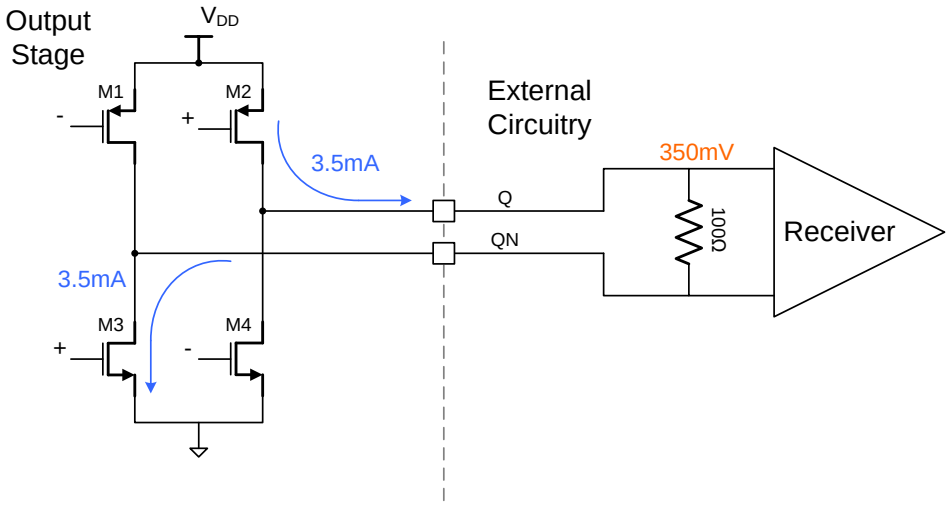
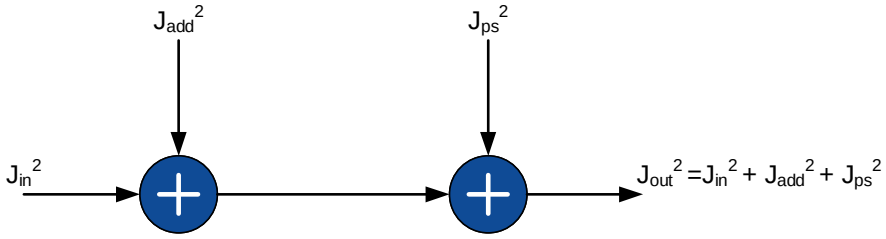


Figure 6 LVDS Termination

Additive Jitter

The AZS15 is not intended to filter clock jitter. The jitter performance of these parts are characterized by its *additive jitter*. Additive jitter is the jitter the device adds to a hypothetical jitter-free clock as it passes through the device. Additive jitter is random and as such it is not correlated to the jitter of the input clock signal.

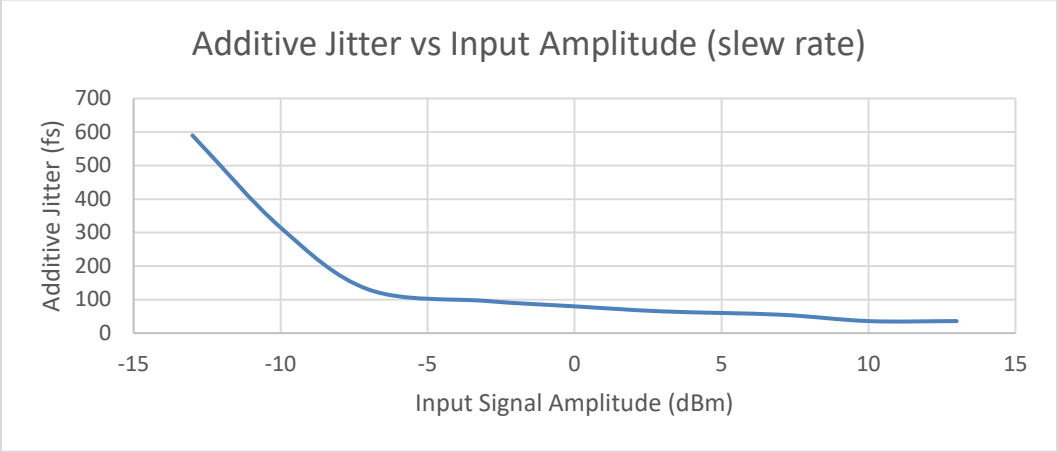
The square of the resultant random RMS jitter at the output is equal to the sum of the squares of the various random RMS jitter sources including: input clock jitter; additive jitter of the buffer; and additive jitter due to power supply noise. The additive jitter of the AZS15 is characterized as the J_{add} term in the following calculation.



J_{in} = Random input clock jitter (RMS)
J_{add} = Additive jitter from device (RMS)
J_{ps} = Additive jitter from power supply noise (RMS)
J_{out} = Resultant random output clock jitter (RMS)

Table 8 Additive Jitter vs Input Amplitude (slew rate)

Input Level (dBm)	Conditions	Additive Jitter	Unit
13	155MHz, 3.3V	36	fs
10	155MHz, 3.3V	36	fs
7	155MHz, 3.3V	55	fs
3	155MHz, 3.3V	65	fs
0	155MHz, 3.3V	80	fs
-3	155MHz, 3.3V	96	fs
-7	155MHz, 3.3V	130	fs
-10	155MHz, 3.3V	315	fs



Single Edge Clock Applications

Certain applications of the AZS10 and AZS15 drive single clock edge sensitive devices such as some analog-to-digital converters. Each edge of the output waveform must be stable without additional added jitter for excellent performance in those applications.

The plot shows the phase noise performance of the AZS10 fed from a 125 MHz low noise oscillator, in a divide by one circuit and an edge sensitive divide by 2 circuit. Edge dependent jitter would show a “hump” in the phase noise curve at 62.5MHz. The phase noise floor is set by the 125 MHz oscillator, and the 1/f noise at 62.5 MHz decreases by 6 dB as expected.

The overlapping phase noise curves show that the buffer does not exhibit edge dependent jitter and will provide excellent performance when driving a single edge sensitive device.

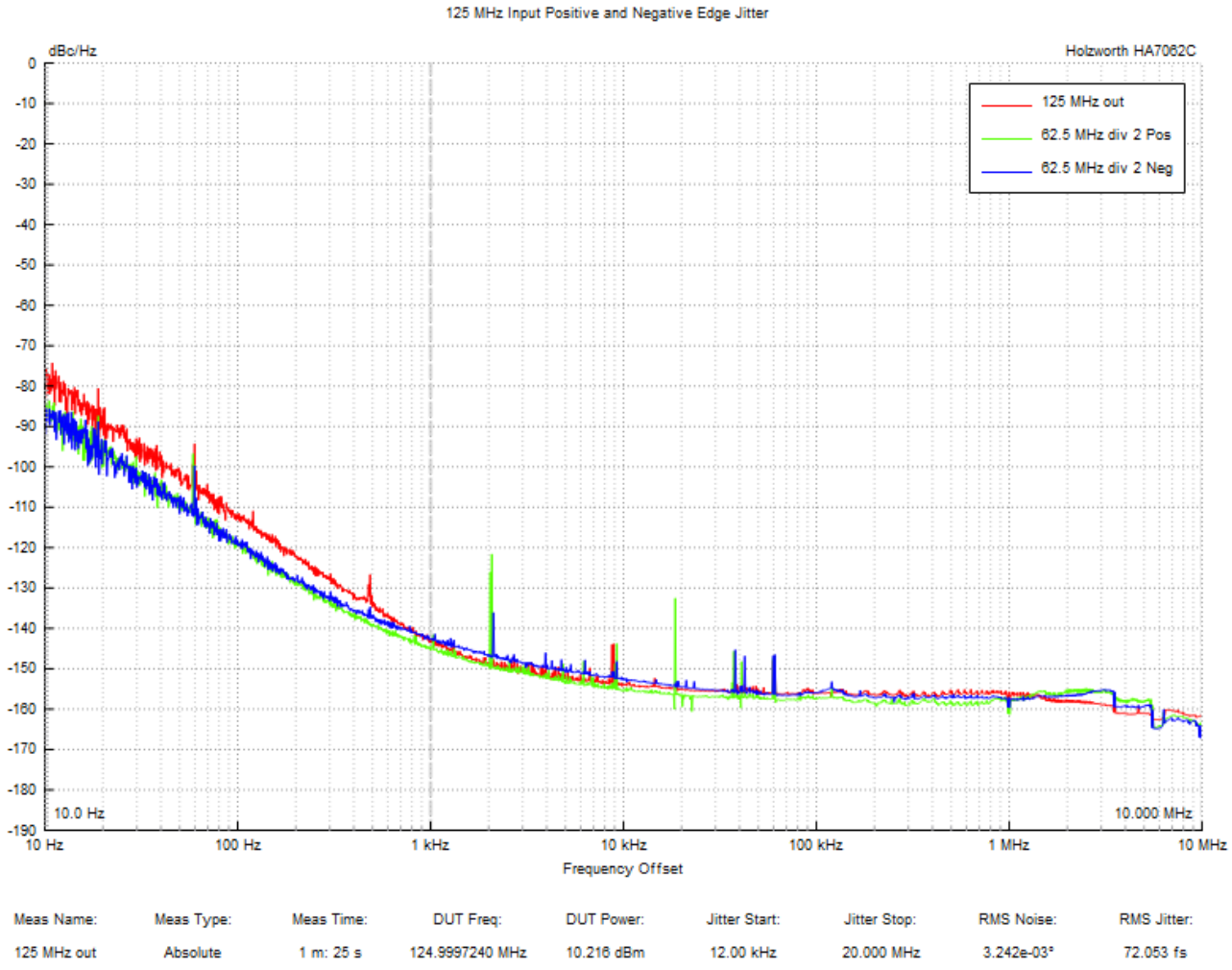


Figure 7 Edge Dependent Jitter

Performance Plots

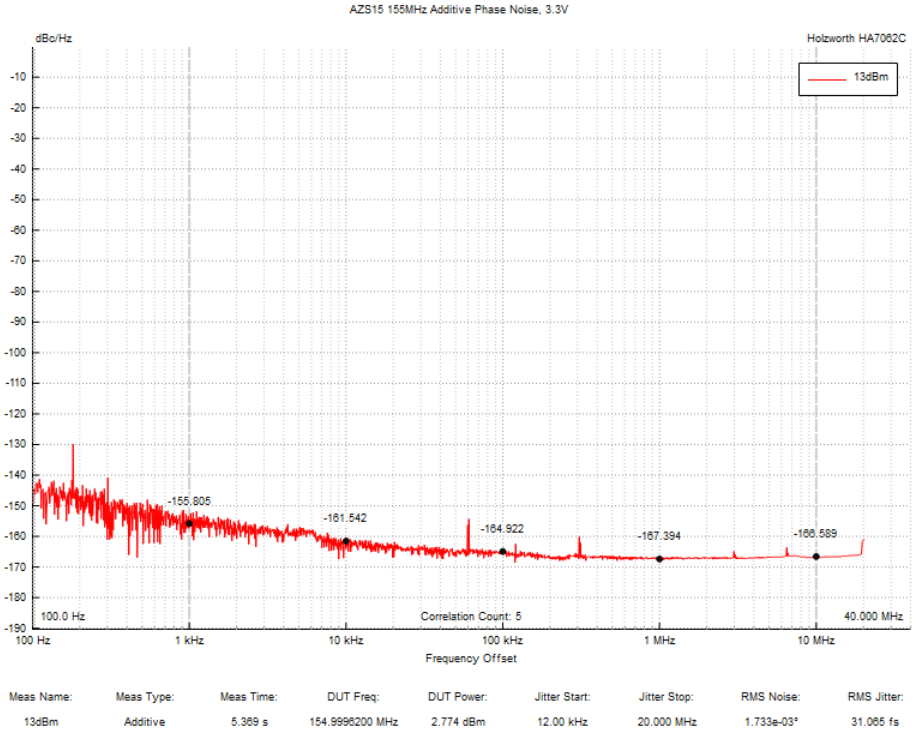


Figure 8 LVPECL Additive Phase Noise, 3.3V

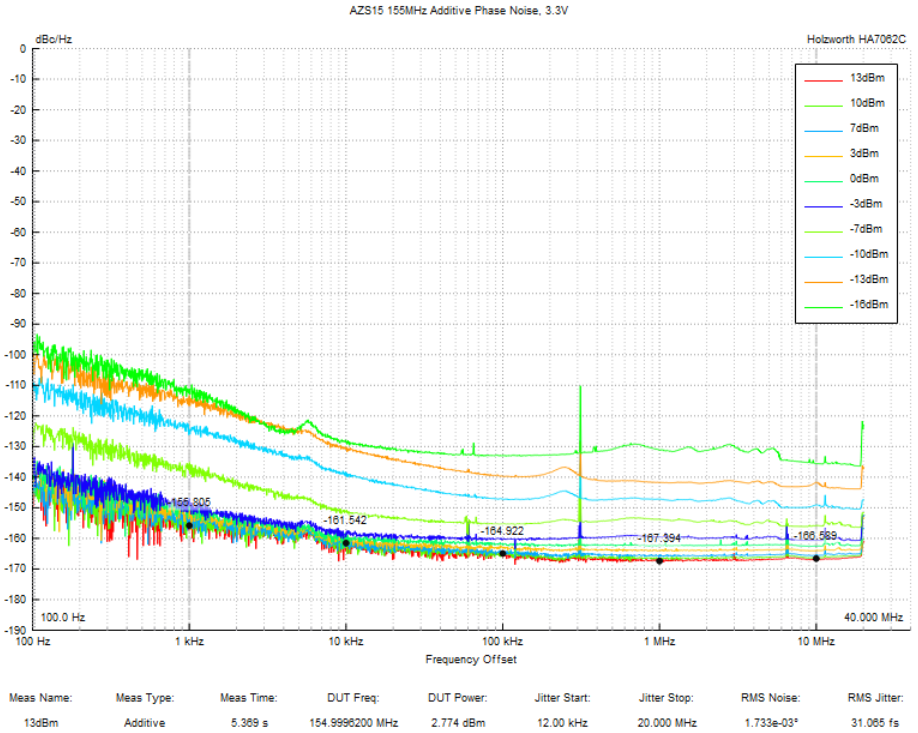


Figure 9 LVPECL Additive Phase Noise vs Input Signal Amplitude, 3.3V

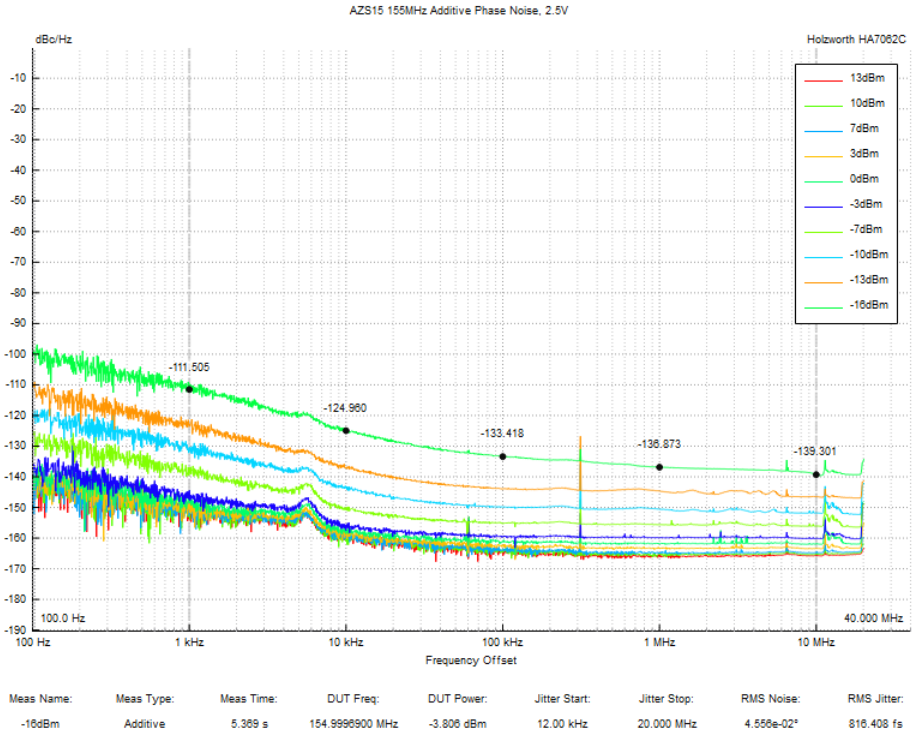


Figure 10 LVPECL Additive Phase Noise vs Input Signal Amplitude, 2.5V

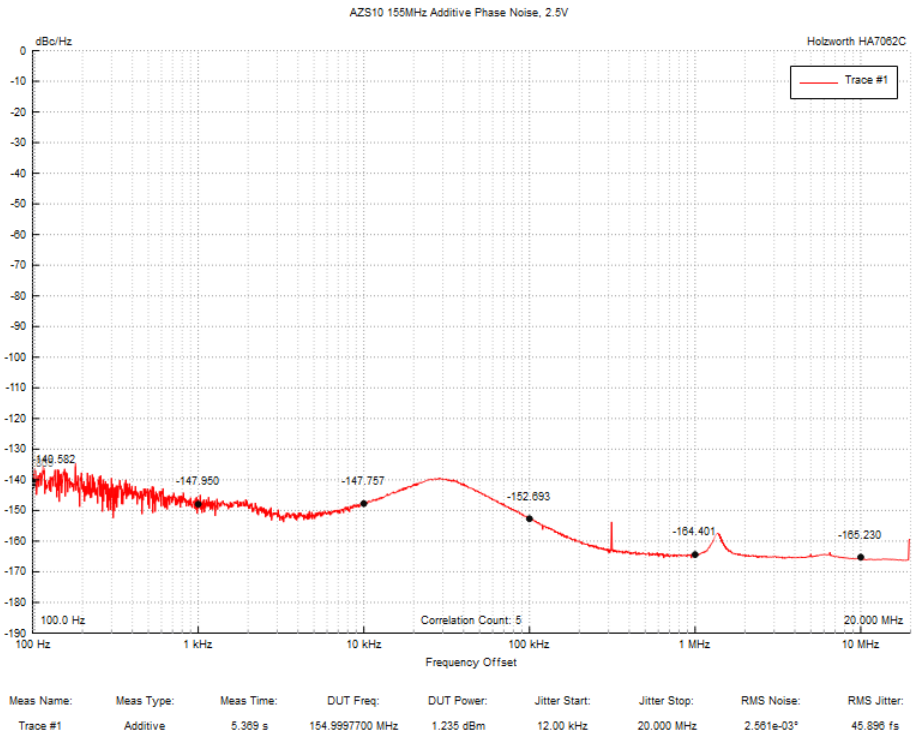


Figure 11 LVDS Additive Phase Noise, 3.3V

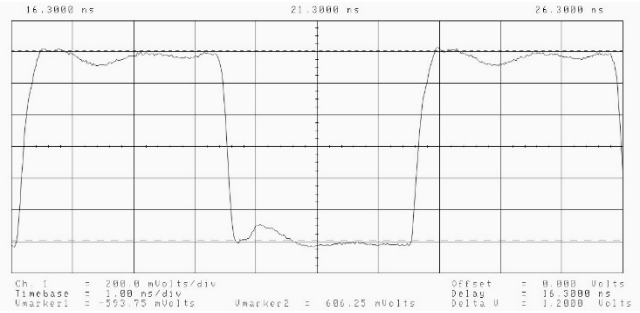


Figure 12 LVPECL 155MHz Output Waveform, 3.3V

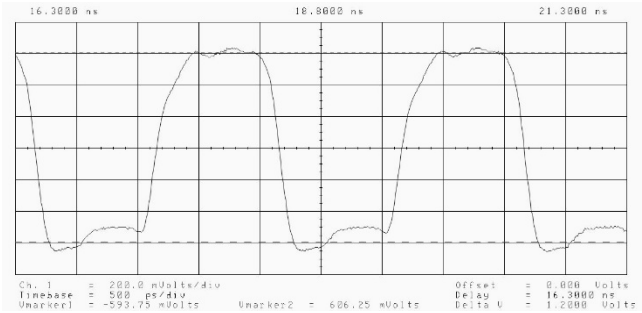


Figure 13 500MHz Output Waveform, 3.3V

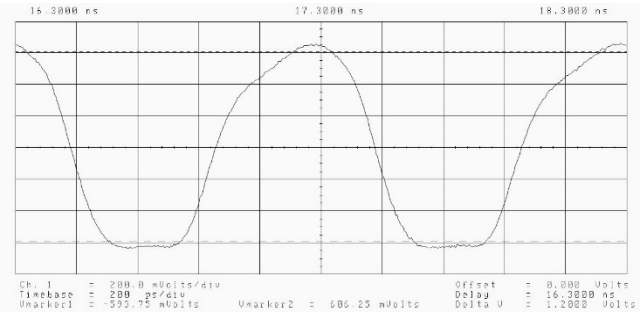


Figure 14 LVPECL 1000MHz Output Waveform, 3.3V

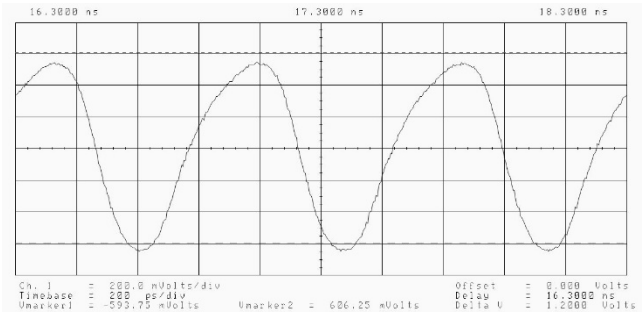


Figure 15 1500MHz Output Waveform, 3.3V

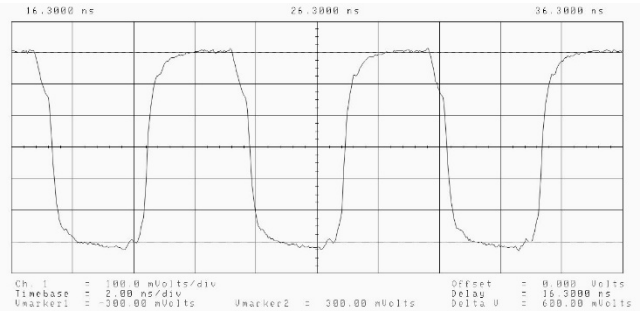


Figure 16 LVDS 155MHz Output Waveform, 3.3V

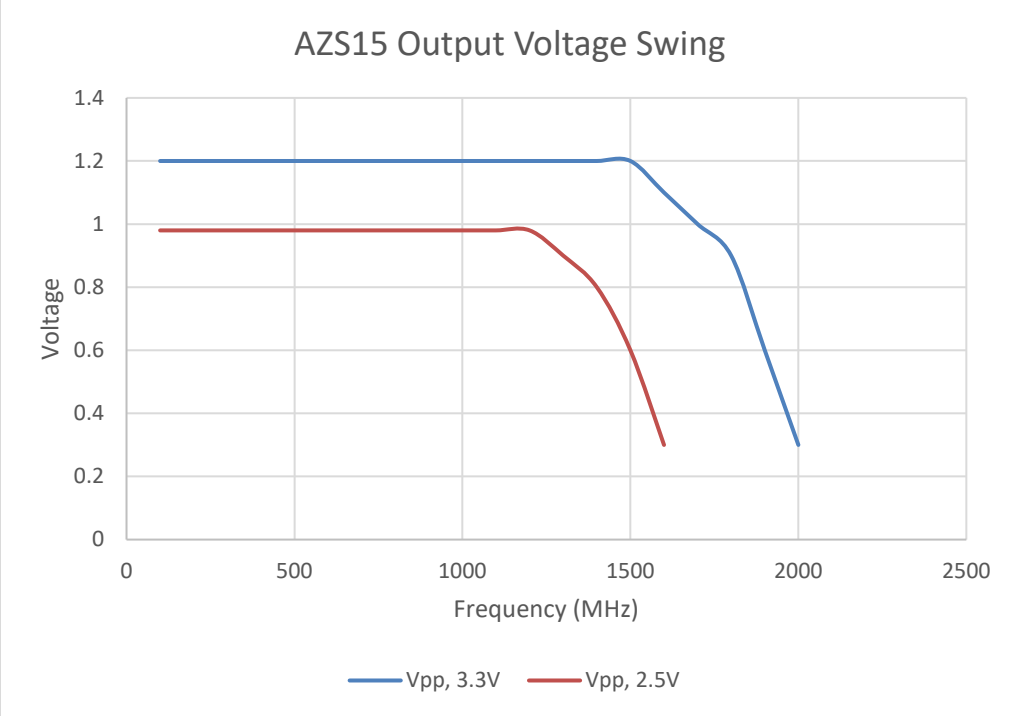


Figure 17 LVPECL Output Swing in Peak to Peak Voltage

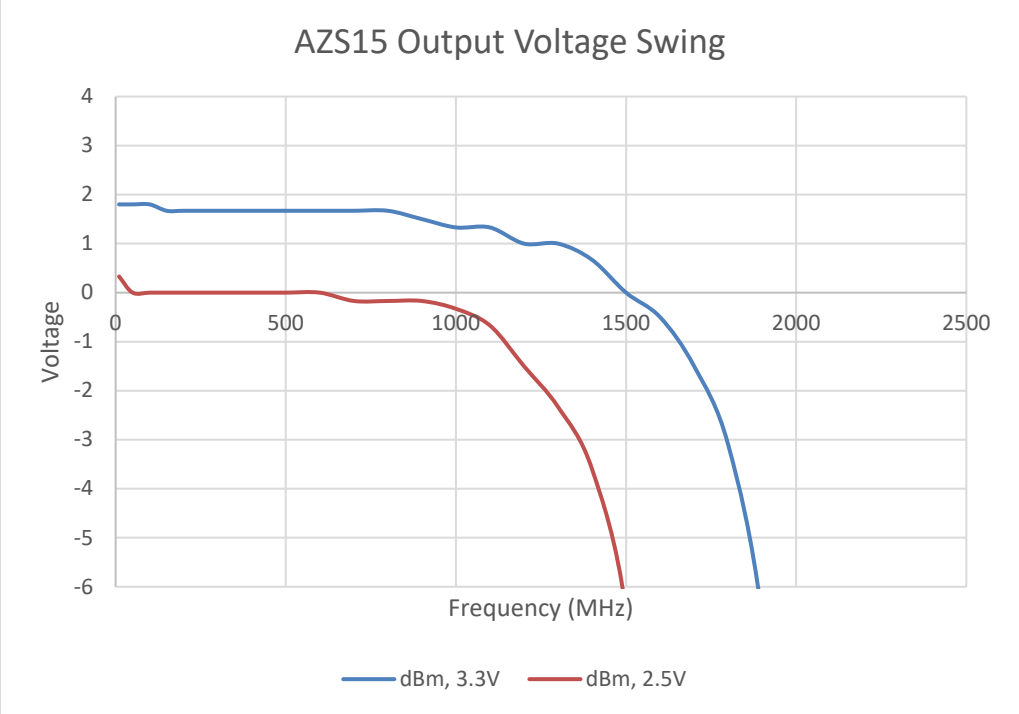
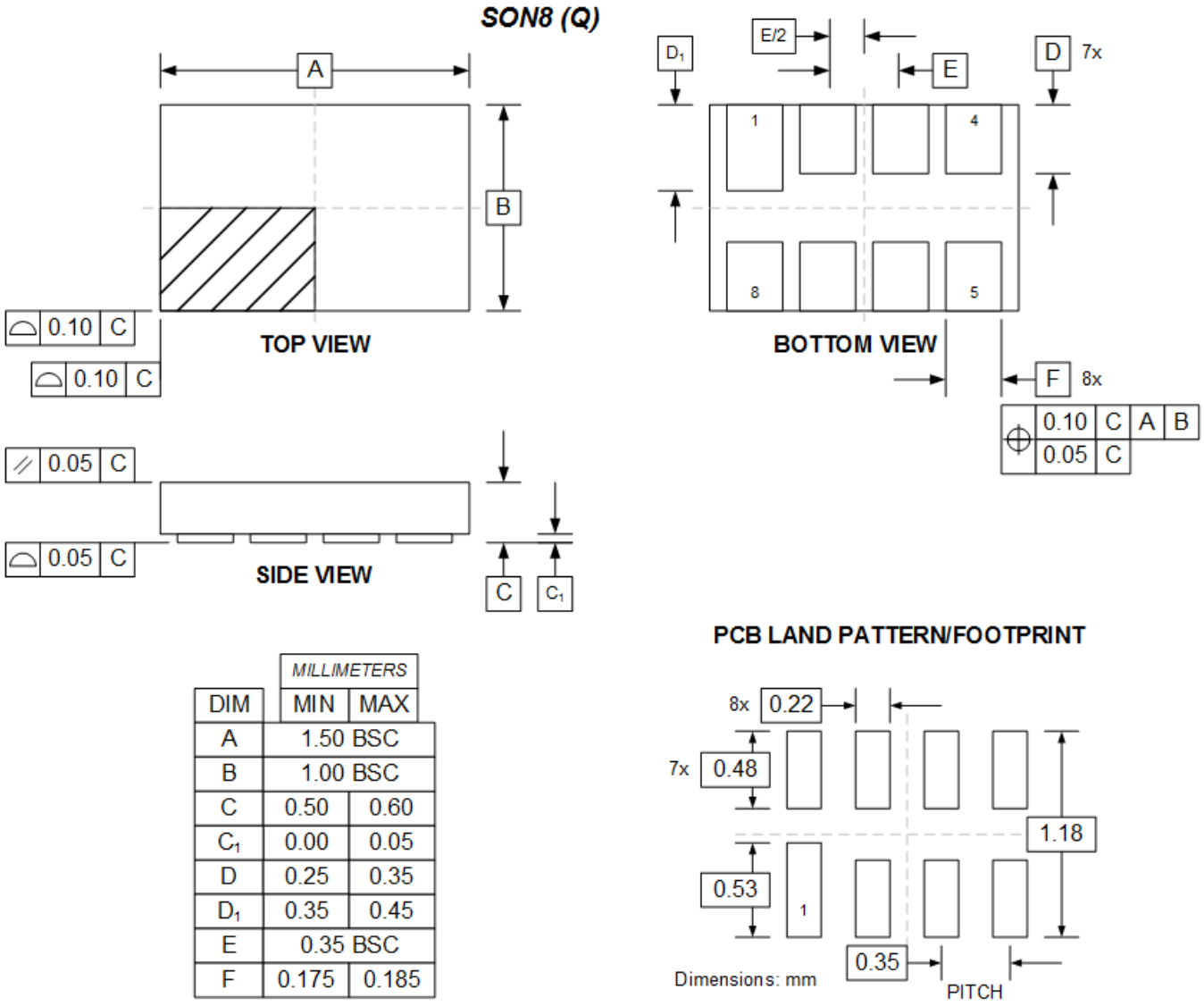


Figure 18 LVPECL Output Swing in dBm

Package Diagrams

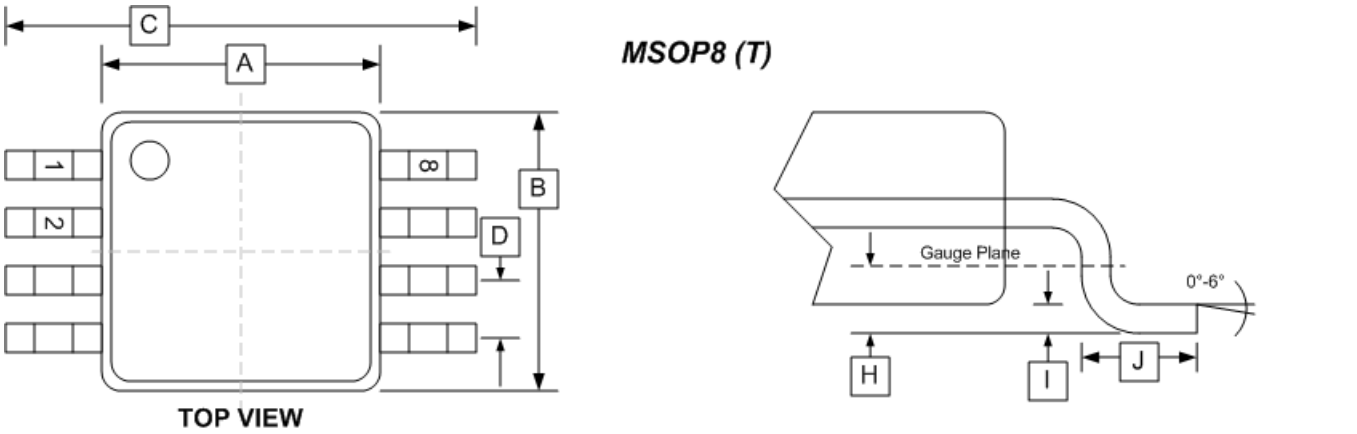
SON8



DIM	MILLIMETERS MIN	MAX
A	1.50 BSC	
B	1.00 BSC	
C	0.50	0.60
C_1	0.00	0.05
D	0.25	0.35
D_1	0.35	0.45
E	0.35 BSC	
F	0.175	0.185

Figure 19 SON8 Package Diagram

MSOP8



	INCHES	
DIM	MIN	MAX
A	0.118±0.004	
B	0.118±0.004	
C	0.192±0.008	
D	0.0256 TYP	
E	0.004±0.002	
F	0.034±0.002	
G	0.009±0.014	
H	0.010	
I	0.006±0.002	
J	0.021±0.004	

Figure 20 MSOP8 Package Diagram

For more information about all of products, please visit our website at
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