Evaluation Board for AZS10 Ultra-Low Phase Noise Buffer & Translator

Description

The AZEBS10 evaluation board is a multi-layer PCB assembly populated with the AZS10 ultra-low phase noise buffer & translator and supporting components. It provides an excellent platform for initial design verification and validation of performance and functionality.

The AZS10 is a configurable LVPECL, LVDS buffer & translator IC that is optimized for ultra-low phase noise and 2.5V & 3.3V nominal supply voltage. It is particularly useful in converting crystal or SAW based oscillators into LVPECL and LVDS outputs for signals up to 1GHz. For designs with very low signal amplitude, consider the AZS15 with a gain stage in the receiver.

The AZS10 is a configurable IC design capable of providing LVPECL or LVDS outputs, ÷1 or ÷2 function, and active high or active low enable selection. See Table 2 for details of the configurations options that provide designers with a single IC buffer/translator solution that is extremely compact, flexible and high performance.

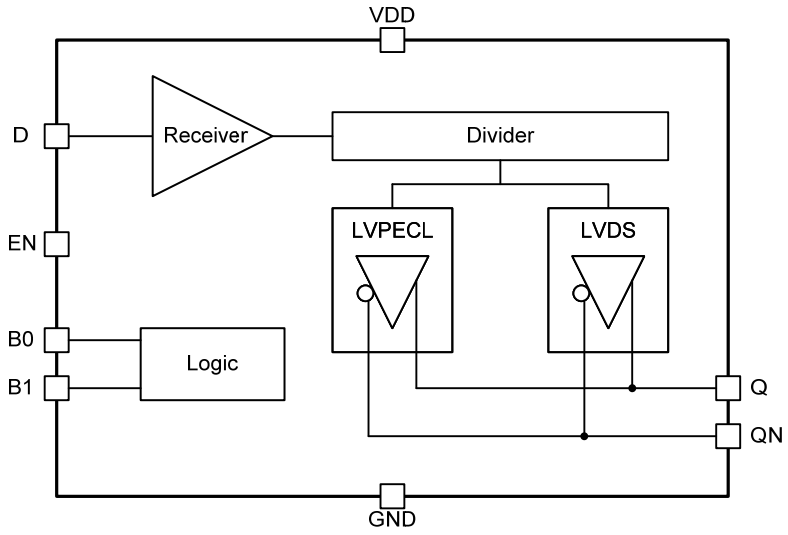
Features

- Ultra-low phase noise floor
  - LVPECL: -167dBc/Hz
  - LVDS: -165dBc/Hz
- Selectable LVPECL/LVDS output levels
- Internal divide by two
- Enable active high or low
- Output frequency up to 1GHz
- Up to 125C operation

Applications

- Crystal or SAW based oscillators
- LVPECL/LVDS clock reference and drivers
- LVPECL/LVDS signal conversion

DUT Block Diagram



Ordering Information

Order Number	DUT Package	Marking
AZS10EVB	SON8	S<date code>

Operation Overview

The AZS10EVB evaluation board is designed to evaluate all the operational modes of the AZS10. Since the output loading is different between LVPECL and LVDS logic levels, two (2) instances of the AZS10 are mounted to the board and have their own independent signal paths (Figure 1). To minimize interface between the DUTs, only one signal path is active at a time and the selection is made through the PECL/LVDS switch.

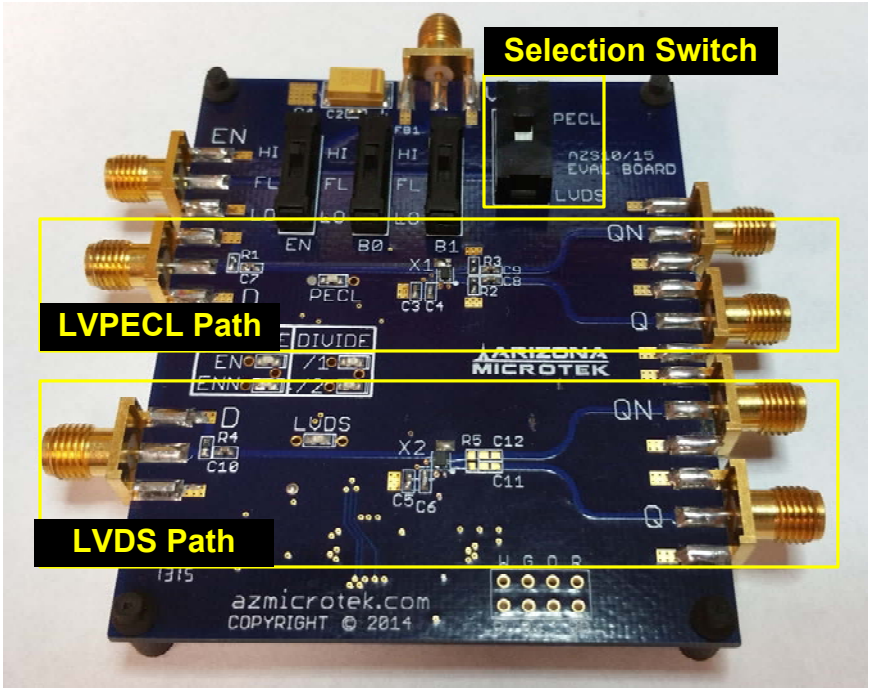


Figure 1

Configuring the operation of the AZS10 is accomplished through the static voltage levels of pins B0 and B1. B0 and B1 are *tri-level inputs* and used to configure the AZS10 into the 8 configurations listed in Table 1.

Table 1

Configuration Bits		Functional Configuration		
B0	**B1**	**Output Type**	**Enable Polarity**	**Output Division**
Open	Open	LVPECL	Active High	÷1
Open	Low	LVPECL	Active High	÷2
Open	High	LVPECL	Active Low	÷1
Low	Open	LVPECL	Active Low	÷2
Low	Low	LVDS	Active High	÷1
Low	High	LVDS	Active High	÷2
High	Open	LVDS	Active Low	÷1
High	Low	LVDS	Active Low	÷2
High	High	not used	not used	not used

The AZS10EVB evaluation board is designed to allow the user to easily move between the possible configurations with the position of the B0 and B1 switches. An additional switch is also added to configure the enable signal into the DUT. The evaluation board also includes LED indicators to help the user identify the current configuration of the DUT.

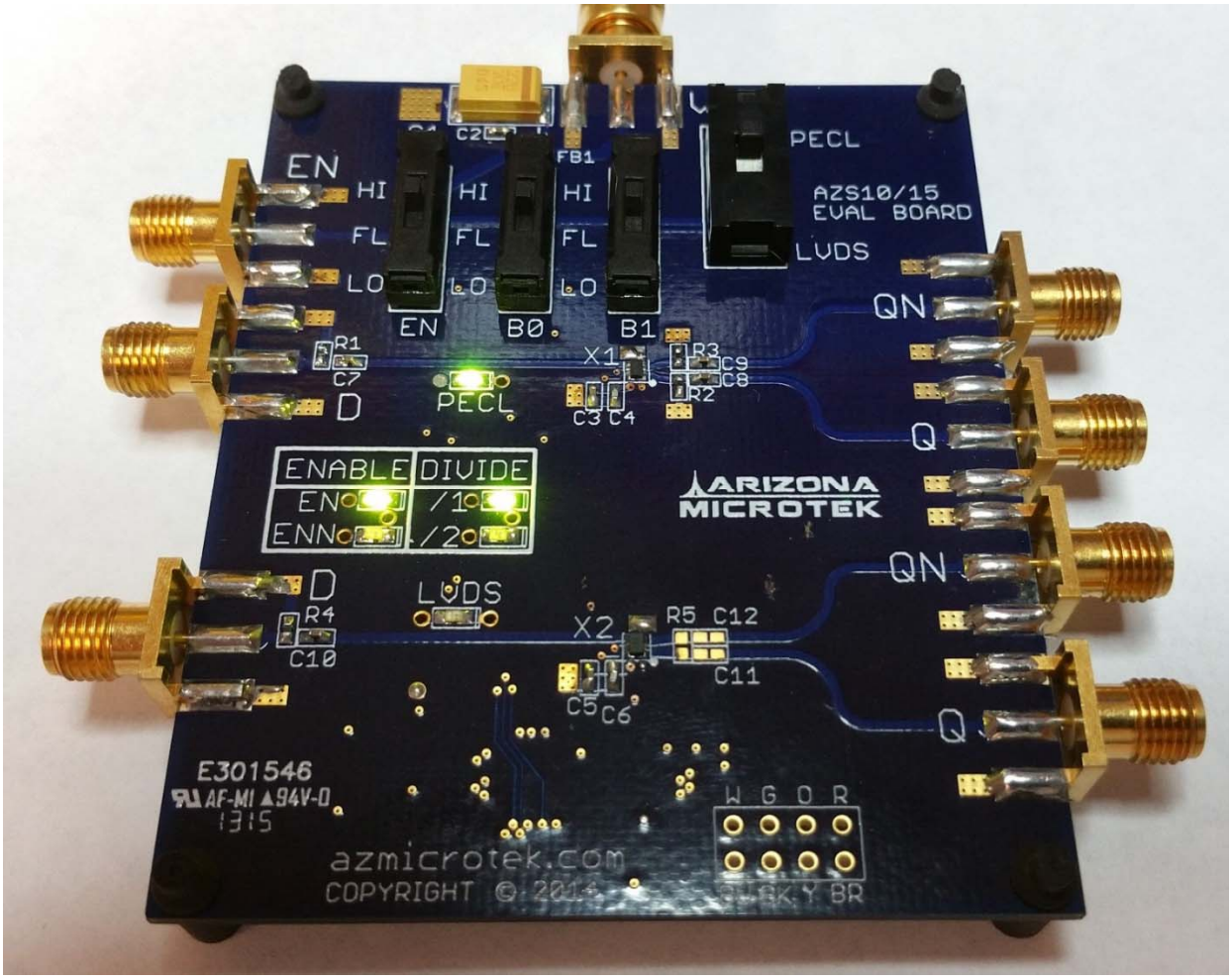


Figure 2

The B0, B1 switches have three possible positions (Hi, Float and Lo) allowing the user to move through the mode configurations listed in Table 1. However, because there is a dedicated PECL/LVDS switch it is possible to put the DUT into an incorrect mode which will then turn all LED indicators off. For example, if the output selection switch is set to PECL, setting the B0 and B1 switches both to LO (an LVDS mode) is invalid.

The EN switch allows the user to enable and disable the DUT without an outside signal source. The AZS10 is capable of being configured to be either active high or active low. If an external enable signal is desired, the EN switch must be placed in the FL position

DUT Input Terminations

The AZS10 input terminal bias is $V_{DD}/2$ fed by an internal 10kΩ resistor. For clock applications, the input signal is AC coupled into the D input to maintain a 50% duty cycle on the outputs. The input can be driven to any voltage between 0V and V_{DD} without damage or waveform degradation.

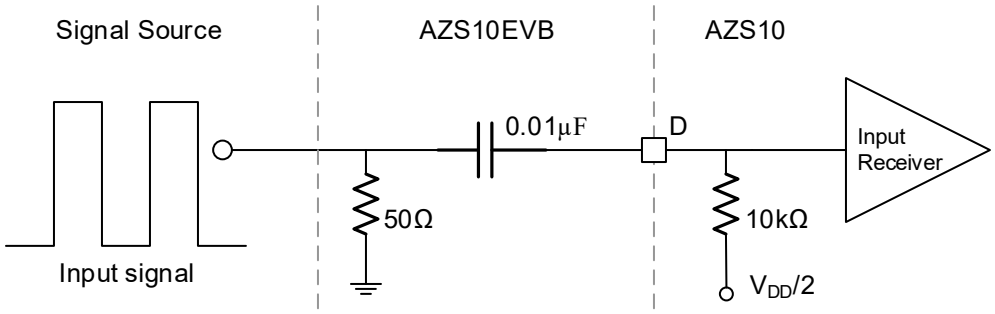


Figure 3

DUT Output Terminations

LVPECL

Most RF and phase noise test sets use AC coupled inputs. Figure 4 shows the AZS10EVB interfacing to test equipment, meeting both DC and AC termination requirements. On-board 100Ω resistors form the DC load. See the AZS10 Application Notes for alternative loading. The test equipment 50Ω input impedance provides the AC termination through C1 and C2.

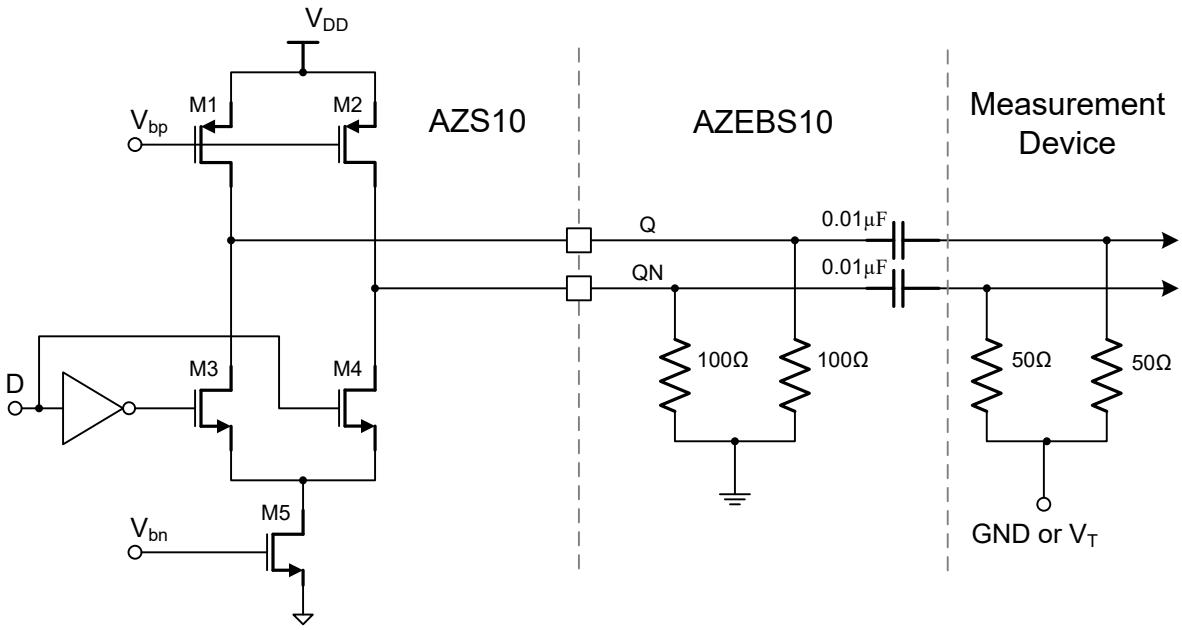


Figure 4 - LVPECL Output Termination

LVDS

The following LVDS termination is compliant to the LVDS specification *TIA/EIA-644A*. By default, the AZS10EVB is configured to have the measurement device provide the correct LVDS loading (Figure 5). Alternatively, LVDS loading can be optionally mounted to the board with the addition of C11, C12 (and cutting the traces around them), and R5 defined in Table 2 and Figure 6.

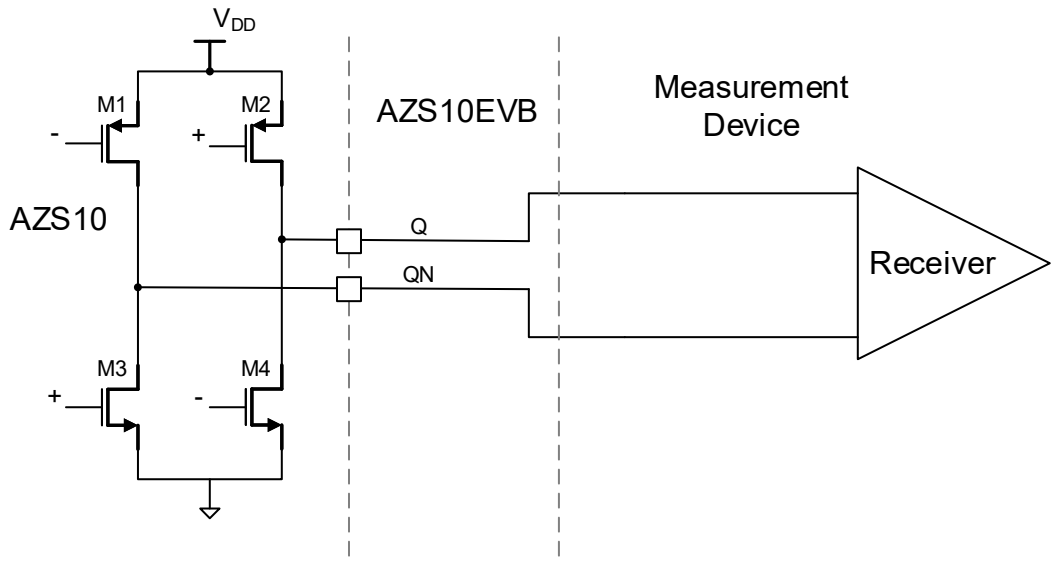


Figure 5 – Default LVDS Output Termination

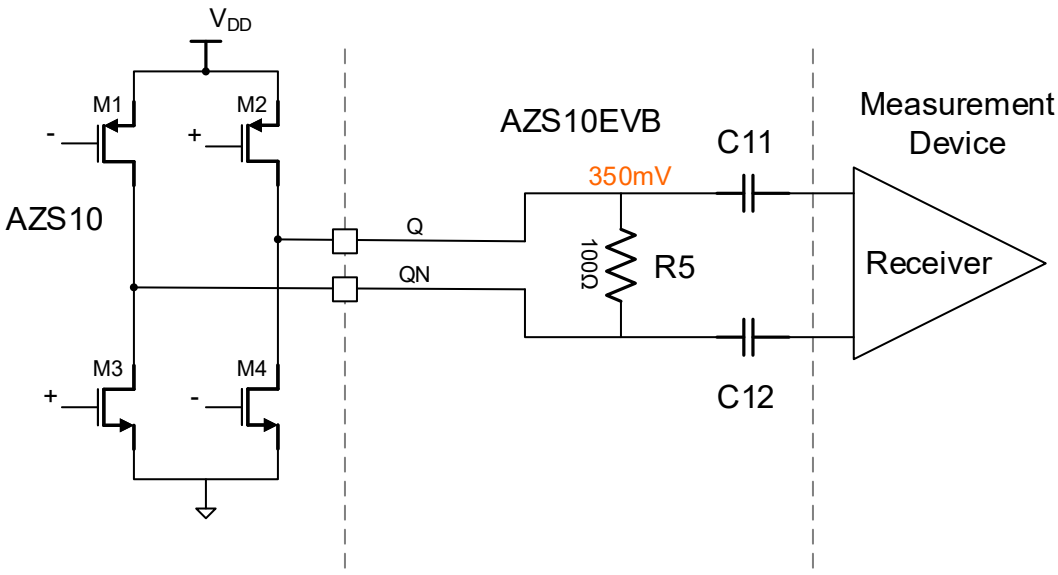


Figure 6 - Optional LVDS Output Termination

Schematic

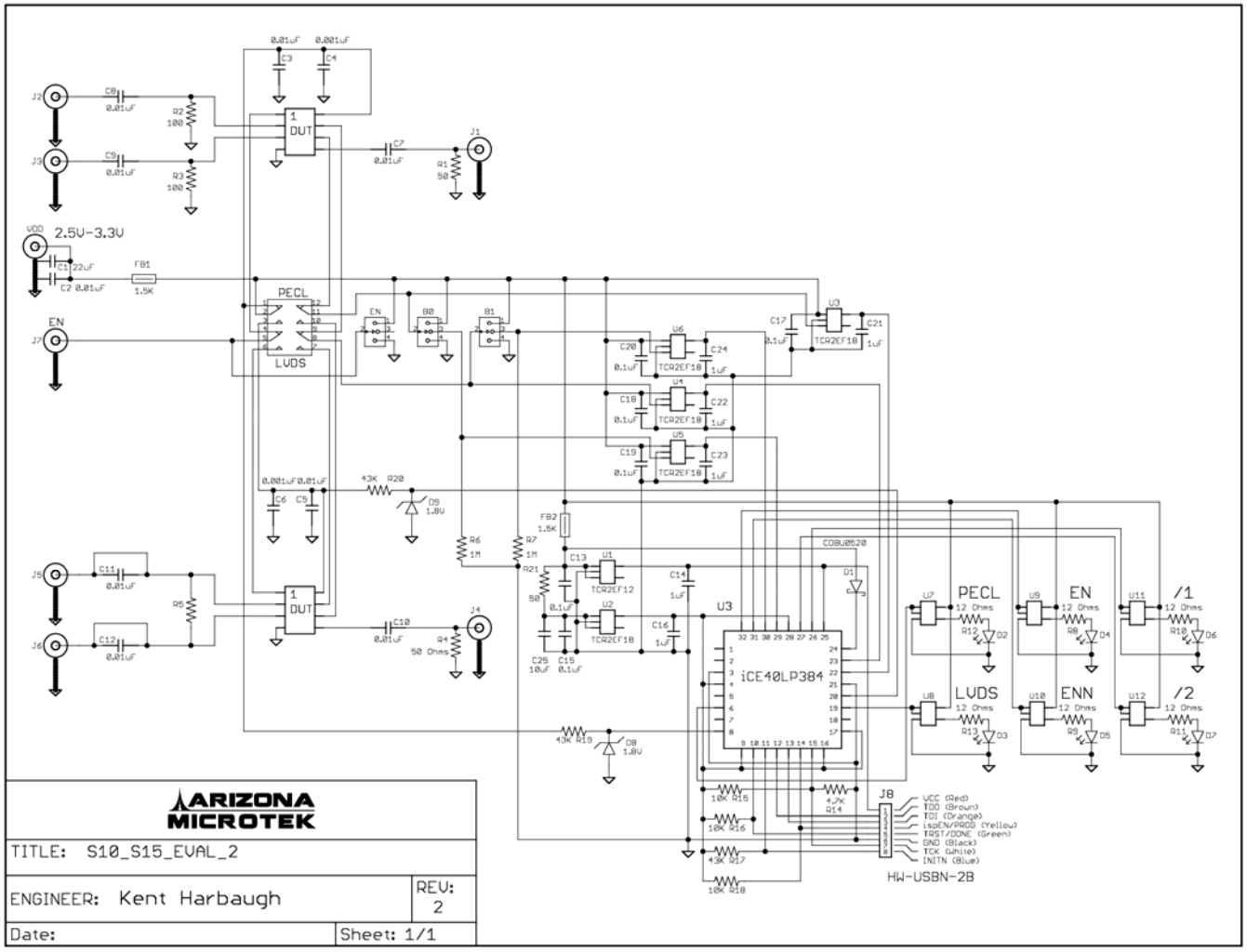


Figure 7

Layout

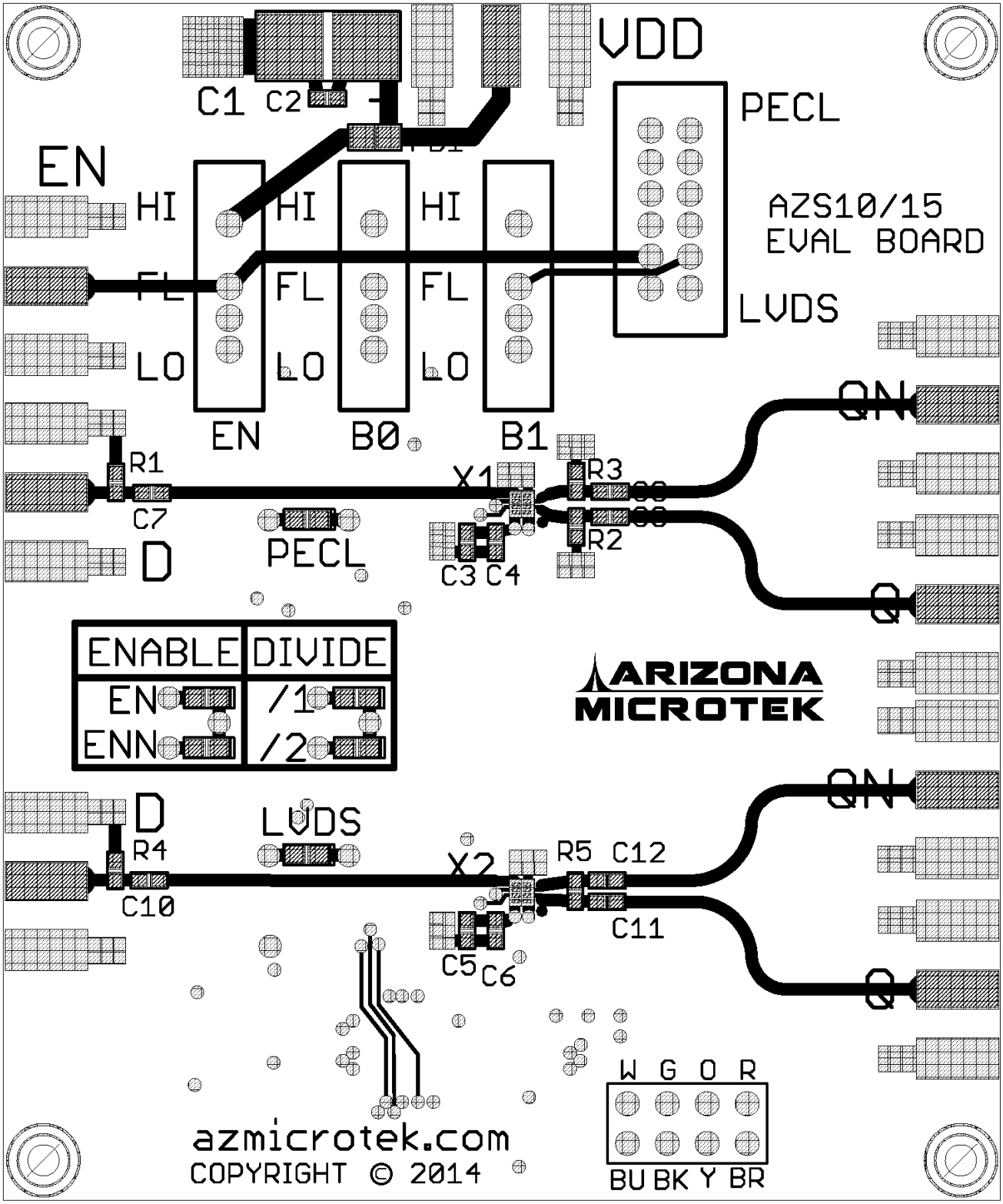


Figure 8

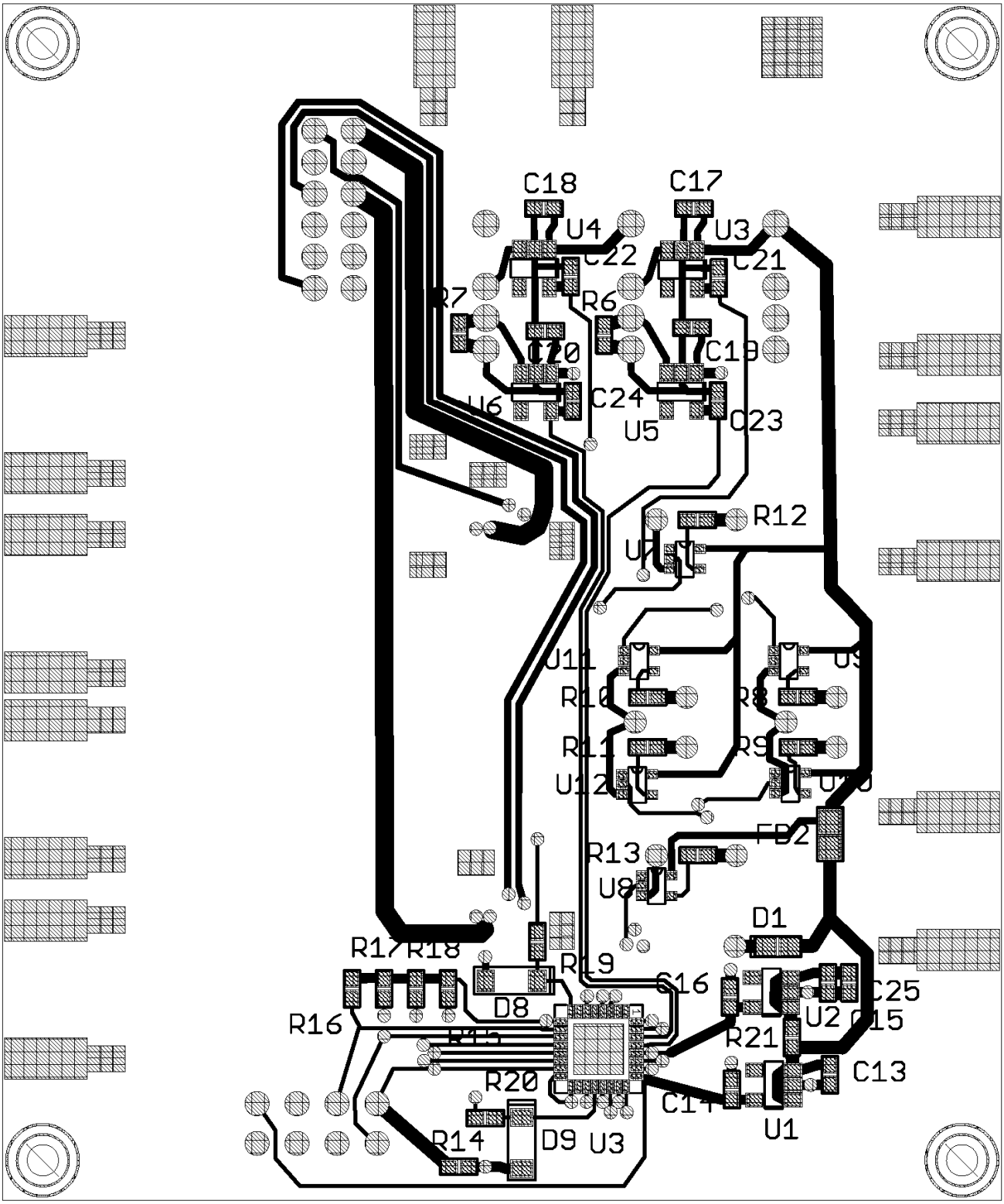

C18
C17
U4
U3
C22
C21
R7
R6
C20
C19
C24
U6
U5
C23
R12
U11
R10
R8
R11
R9
U12
FB2
R13
U8
D1
R17
R18
R19
C16
C25
D8
U2
R16
R21
C15
C13
R20
C14
U1
R14
D9
U3

Figure 9

BOM

Table 2

Item	REF #	QTY	Description	Case
1	C1	1	22uF 16V 10% Tant Cap	2917 SMT
2	C2, C3, C5, C7, C8, C9, C10, ~~C11, C12~~	9	10000pF 50V 10% Cer Cap	0402 SMD
3	C4, C6	2	1000pF 50V 5% Cer Cap	0402 SMD
4	C13, C15, C17, C18, C19, C20	6	0.1uF 50V 10% Cer Cap	0402 SMD
5	C14, C16, C21, C22, C23, C24	6	1uF 50V 5% Cer Cap	0402 SMD
6	C25, C26	2	10uF 10V 20% Cer Cap	0402 SMD
7	R1, R4, R21, R22	4	49.9Ω 1/10W 1% Res	0402 SMD
8	R2, R3, ~~R5~~	3	100Ω 1/10W 1% Res	0402 SMD
9	R6, R7	2	1MΩ 1/10W 1% Res	0402 SMD
10	R8, R9, R10, R11, R12, R13	6	12Ω 1/10W 1% Res	0402 SMD
11	R14	1	4.7KΩ 1/10W 1% Res	0402 SMD
12	R15, R16, R18	3	10KΩ 1/10W 1% Res	0402 SMD
13	R17, R19, R20	3	43KΩ 1/10W 1% Res	0402 SMD
14	FB1, FB2	2	FERRITE CHIP 2.7KΩ 200mA	0805 SMD
15	U1	1	1.2V LDO	SOT23-5
16	U2, U3, U4, U5, U6	5	1.8V LDO	SOT23-5
17	U7, U8, U9, U10, U11, U12	6	AND GATE	SC70-5
18	D1	1	Schottky Diode	0603 SMD
19	D2 (PECL), D3 (LVDS), D4 (EN), D6 (/1)	4	Green LED	0603 SMD
20	D5 (ENN), D7(/2)	2	Yellow LED	0603 SMD
20 alt	D5 (ENN), D7(/2)	2	Orange LED	0603 SMD
21	D8, D9	2	1.8V Zender Diode	SOD123
22	X1, X2	2	AZS10QG (DUT)	8SON 1.5x1.0
23	J1, J2, J3, J4, J5, J6, J7, J8	8	SMA FEMALE EDGE	EDGE MNT
24	U13	1	FPGA	QFN32
25	PECL / LVDS	1	4PDT SLIDE SWITCH	PCB THRU HOLE
26	B0, B1, EN	3	SP3T SLIDE SWITCH	PCB THRU HOLE
27	STANDOFF	4	RUBBER STANDOFF	PCB THRU HOLE
28	J9	1	1x6 FLYWIRE HEADER	PCB THRU HOLE
29	AZEBS10-1	1	BLANK PCB	N/A
	ASSEMBLY	1	N/A	N/A

Revision History

Revision	Date	Description
1.0	4/9/14	Initial Release
2.0	10/1/15	New evaluation board revision
2.1	3/13/17	Updated typos

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