AZ100EL16VO

LVPECL Oscillator Gain Stage & Buffer with Enable

www.azmicrotek.com

DESCRIPTION

The AZ100EL16VO is an oscillator gain stage with a high gain output buffer including an enable. The $Q_{HG}/\overline{Q}_{HG}$ outputs have a voltage gain several times greater than the Q/$\overline{Q}$ outputs. An enable input ($\overline{EN}$) allows continuous oscillator operation. The enable can be controlled by ECL or CMOS signals

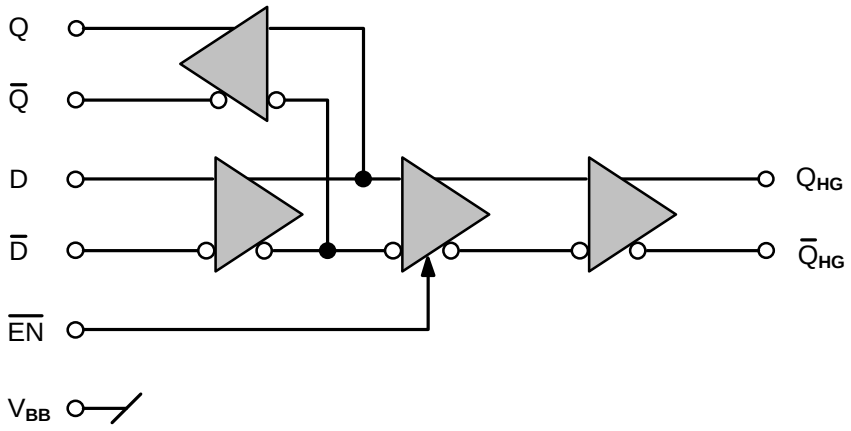
FEATURES

- 250ps propagation delay
- High voltage gain vs. standard EL16
- 75kΩ enable pull-down Resistor
- High bandwidth for ≥1GHz
- -147 dBc/Hz typical noise floor

APPLICATIONS

- Crystal or SAW oscillators

BLOCK DIAGRAM



PACKAGE AVAILABILITY

- MLP8
- MLP16
- MSOP8
- MSOP10
- Green/RoHS Compliant/Pb-Free

Order Number	Package	Marking
AZ100EL16VONG[1]	MLP8	P0G / <Date Code>[2]
AZ100EL16VONBG[1]	MLP8	P4G / <Date Code>[2]
AZ10/100EL16VOLG[1]	MLP16	AZMG / 16J / <Date Code>[2]
AZ100EL16VOTG[1]	MSOP8	HVOG / <Date Code>[2,3]
AZ100EL16VOTFG[1]	MSOP8	HVOFG / <Date Code>[2]
AZ100EL16VOUG[1]	MSOP10	HVOUG / <Date Code>[2,4]

[1] Tape & Reel - Add 'R1' at end of order number for 7in (1k parts), 'R2' (2.5k) for 13in

[2] See www.azmicrotek.com for date code format

[3] Date code 141 and earlier on belly mark, AZH+ / 16VO on top

[4] Date code 0633 and earlier on belly mark, AZH+ / 16VOU on top

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PIN DESCRIPTION AND CONFIGURATION

Table 1 - Pin description for MLP8 (AZ100EL16VON) package

Pin	Name	Type	Function
1	$\overline{Q}$	Output	Inverting PECL Output
2	D	Input	Data Input
3	V_{BB}	Output	Reference Voltage
4	$\overline{EN}$	Input	Output Enable
5	V_{EE}	Power	Negative Supply
6	$\overline{Q}_{HG}$	Output	High Gain Inverting PECL Output
7	Q_{HG}	Output	High Gain PECL Output
8	V_{CC}	Power	Positive Supply

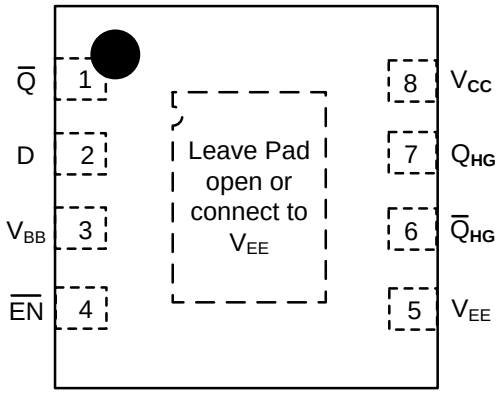


Figure 1 – Pin configuration for AZ100EL16VON (MLP8)

Table 2 - Pin description for MLP8 (AZ100EL16VONB) package

Pin	Name	Type	Function
1	D	Input	Data Input
2	V_{BB}	Output	Reference Voltage
3	$\overline{EN}$	Input	Output Enable
4	V_{EE}	Power	Negative Supply
5	$\overline{Q}_{HG}$	Output	High Gain Inverting PECL Output
6	Q_{HG}	Output	High Gain PECL Output
7	V_{CC}	Power	Positive Supply
8	$\overline{Q}$	Output	Inverting PECL Output

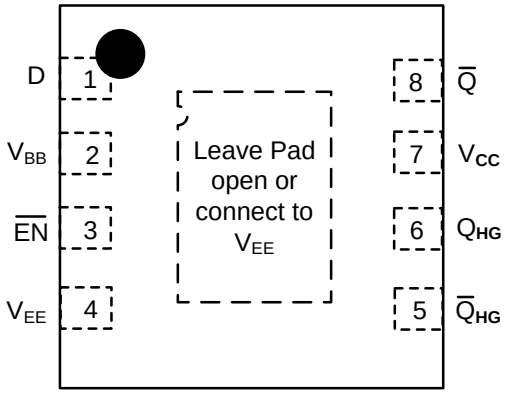


Figure 2 – Pin configuration for AZ100EL16VONB (MLP8)

Table 3 - Pin description for MSOP8 (AZ100EL16VOT) package

Pin	Name	Type	Function
1	$\overline{Q}$	Output	Inverting PECL Output
2	D	Input	Data Input
3	V_{BB}	Output	Reference Voltage
4	$\overline{EN}$	Input	Output Enable
5	V_{EE}	Power	Negative Supply
6	$\overline{Q}_{HG}$	Output	High Gain Inverting PECL Output
7	Q_{HG}	Output	High Gain PECL Output
8	V_{CC}	Power	Positive Supply

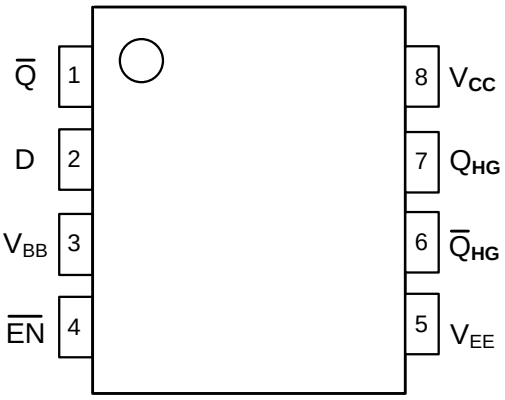


Figure 3 – Pin configuration for AZ100EL100VOT (MSOP8)

Table 4 - Pin description for MSOP8 (AZ100EL16VOTF) package

Pin	Name	Type	Function
1	$\overline{Q}$	Output	Inverting PECL Output
2	D	Input	Data Input
3	$\overline{D}$	Input	Inverting Data Input
4	$\overline{EN}$	Input	Output Enable
5	V_{EE}	Power	Negative Supply
6	$\overline{Q}_{HG}$	Output	High Gain Inverting PECL Output
7	Q_{HG}	Output	High Gain PECL Output
8	V_{CC}	Power	Positive Supply

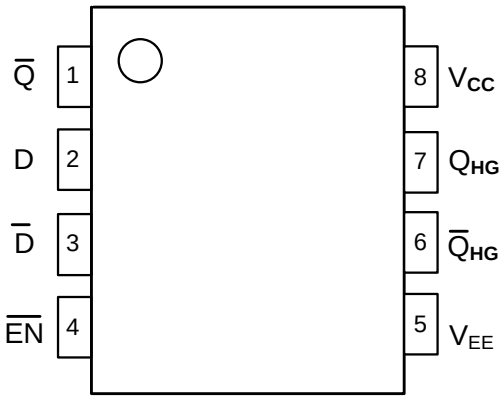


Figure 4 – Pin configuration for AZ100EL100VOTF (MSOP8)

Table 5 - Pin description for MSOP10 package

Pin	Name	Type	Function
1	Q	Output	PECL Output
2	$\overline{Q}$	Output	Inverting PECL Output
3	D	Input	Data Input
4	$\overline{D}$	Input	Inverting Data Input
5	V_{BB}	Output	Reference Voltage
6	$\overline{EN}$	Input	Output Enable
7	V_{EE}	Power	Negative Supply
8	$\overline{Q}_{HG}$	Output	High Gain Inverting PECL Output
9	Q_{HG}	Output	High Gain PECL Output
10	V_{CC}	Power	Positive Supply

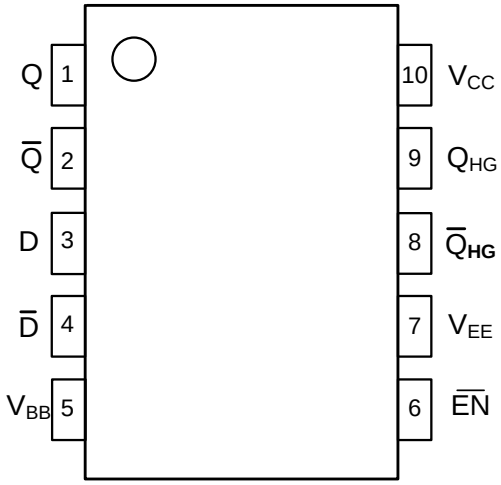
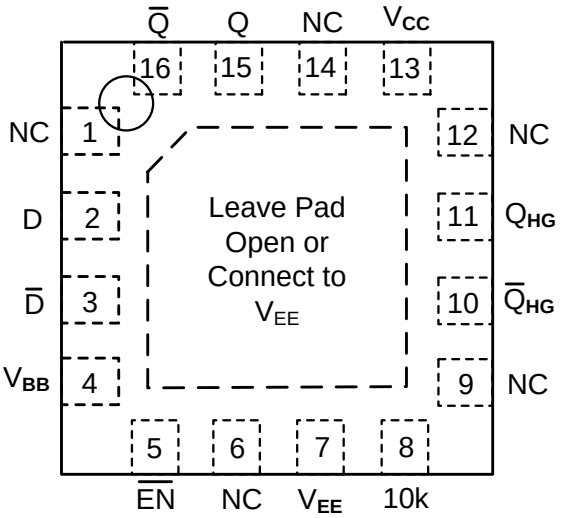


Figure 5 - Pin configuration for AZ100EL16VOU (MSOP10)

Table 6 - Pin description for MLP16 package

Pin	Name	Type	Function
1	NC		
2	D	Input	Data Input
3	$\overline{D}$	Input	Inverting Data Input
4	V_{BB}	Output	Reference Voltage
5	$\overline{EN}$	Input	Output Enable
6	NC		
7	V_{EE}	Power	Negative Supply
8	10k	Input	10k Enable
9	NC		
10	$\overline{Q}_{HG}$	Output	High Gain Inverting PECL Output
11	Q_{HG}	Output	High Gain PECL Output
12	NC		
13	V_{CC}	Power	Positive Supply
14	NC		
15	Q	Output	PECL Output
16	$\overline{Q}$	Output	Inverting PECL Output



ENGINEERING NOTES

The AZ100EL16VO is an oscillator gain stage with a high gain output buffer including an enable. The $Q_{HG}/\overline{Q}_{HG}$ outputs have a voltage gain several times greater than the $Q/\overline{Q}$ outputs. An enable input ($\overline{EN}$) allows continuous oscillator operation. When $\overline{EN}$ is LOW or floating (NC), input data is passed to both sets of outputs. When $\overline{EN}$ is HIGH, the $Q_{HG}/\overline{Q}_{HG}$ outputs will be forced LOW/HIGH respectively, while input data will continue to be passed to the $Q/\overline{Q}$ outputs. The $\overline{EN}$ input can be driven with an ECL/PECL signal or a CMOS logic signal.

The input impedance of the $D/\overline{D}$ inputs remain constant for all operating modes since forcing the outputs via the $\overline{EN}$ pin does not power-down the chip but only disables the high gain $Q_{HG}/\overline{Q}_{HG}$ outputs.

Input protection diodes are included on the $D/\overline{D}$ inputs for enhanced ESD protection.

The AZ100EL16VO also provides a V_{BB} output that supports 1.5mA sink/source current. When used, the V_{BB} pin should be bypassed to ground or V_{CC} via a 0.01µF capacitor.

Any used output must have an external pull down resistor. For 3.3V operation, an 180Ω resistor to V_{EE} is recommended if an AC coupled load is present. At 5.0V, a 330Ω resistor is recommended for the AC load case. Alternately, a 50Ω load terminated to V_{CC} – 2V or the Thevenin equivalent may be driven directly. Unused outputs may be left floating (NC).

10k temperature compensation is offered on the AZ100LVEL16VOL. If this mode is desired, connect the 10k pin to V_{EE}. The connection must be less than 1Ω.

NOTE: Specifications in ECL/PECL tables are valid when thermal equilibrium is established.

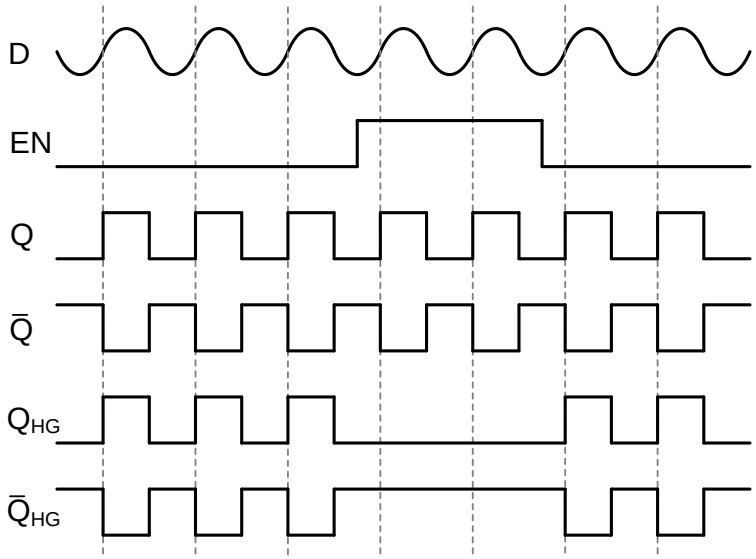


Figure 7 - AZ100EL16VO Timing Diagram

Table 7 - Enable Truth Table

$\overline{EN}$	$Q/\overline{Q}$	Q_{HG}	$\overline{Q}_{HG}$
LOW or NC	Data	Data	Data
HIGH	Data	LOW	HIGH

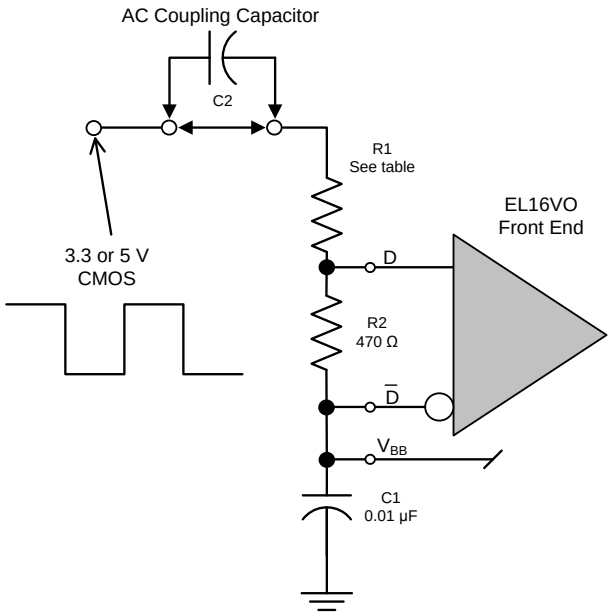


Figure 8 – Application circuit for CMOS Inputs

Table 8 – Recommended Component Values for CMOS Single Ended Inputs

Input Type	R1[1] Value	
	AC Coupled (C2 in circuit)	DC Coupled (C2 shorted)
3.3V CMOS	430Ω	750Ω
5.0V CMOS	910Ω	1.8kΩ

1. R1 should be chosen so that the input swing on the D input with respect to $\overline{D}$ is in the range of ±80 to ±1000 mV, per the AC Characteristics table and the D input is < ±750 mV with respect to V_{BB}.

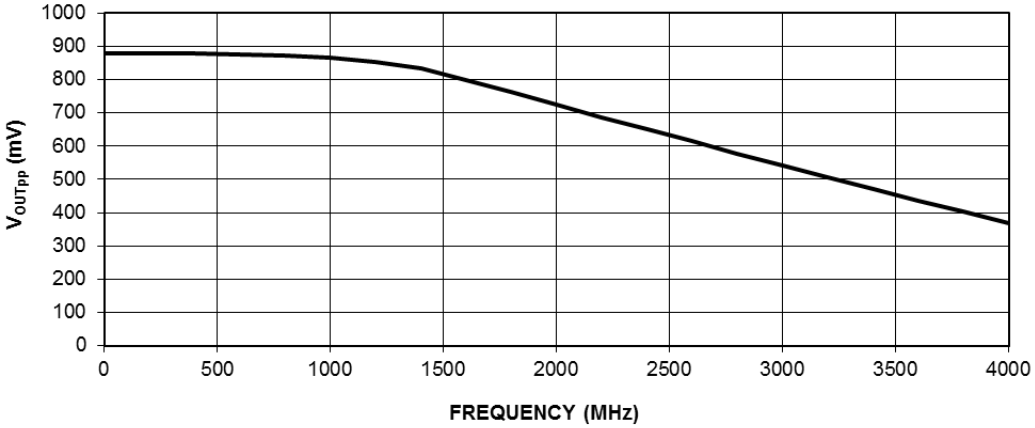


Figure 9 – Typical Large Signal Output Swing

Measured with 750mv differential input, V_{EEP} NC, $Q_{HG}/\overline{Q}_{HG}$ each terminated to V_{CC}-2V via 50 Ω resistors.

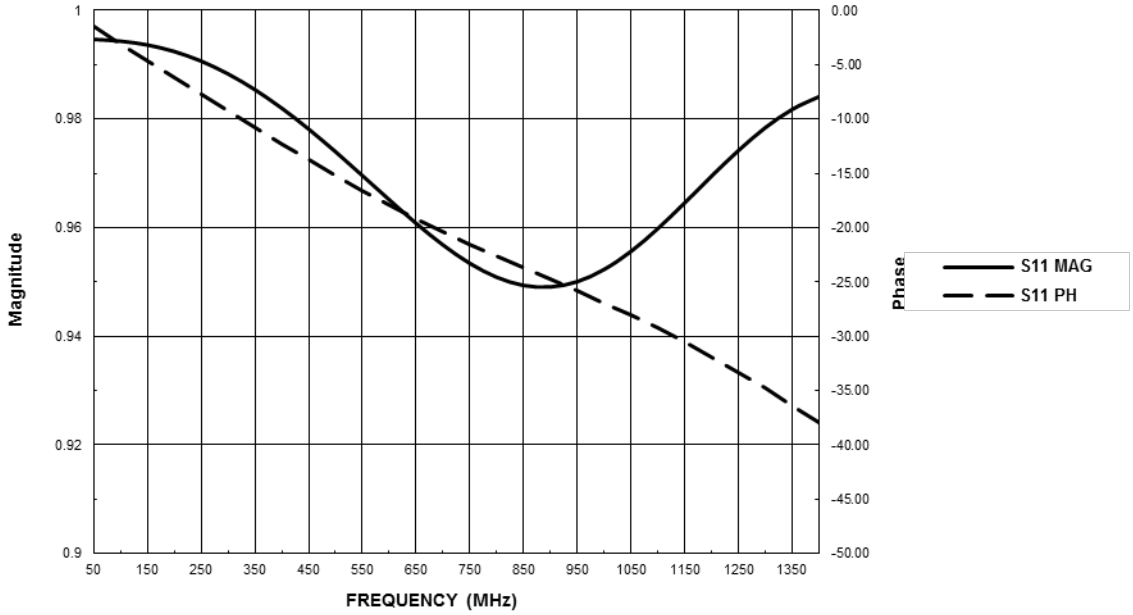


Figure 10 - S11, 50Ω load to V_{CC} - 2V

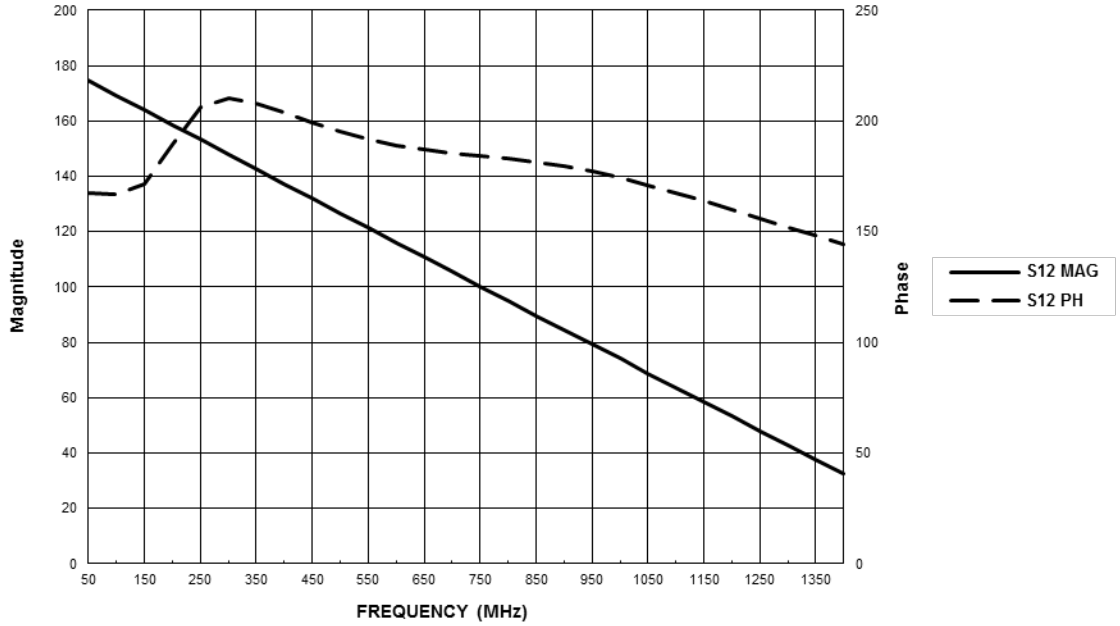


Figure 11 - S12, 50Ω load to V_{CC} - 2V

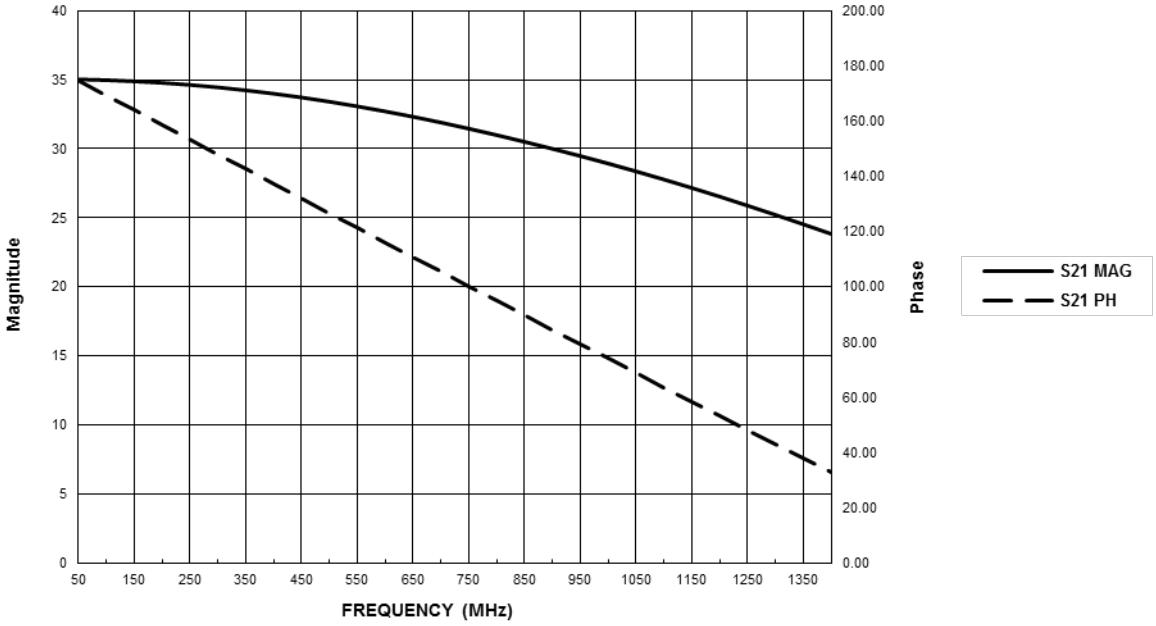


Figure 12 – S21, 50Ω load to V_{CC} - 2V

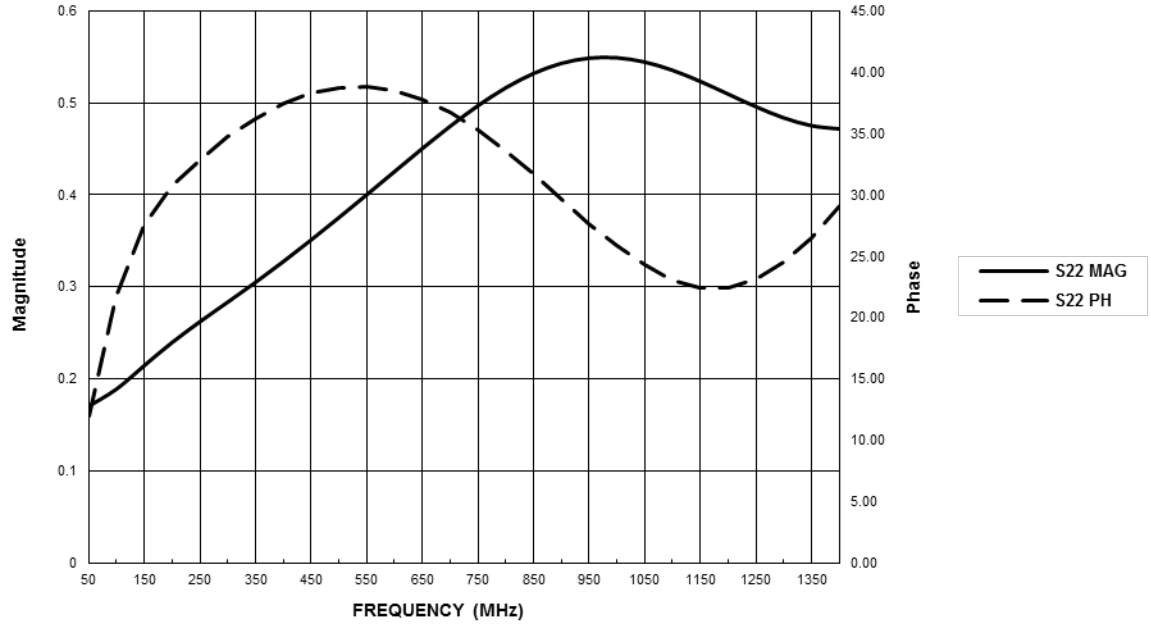


Figure 13 - S22, 50Ω load to V_{CC} - 2V

PERFORMANCE DATA

Table 9 – Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	V_{EE} = 0V	0 to + 6.0	V
V_{I_PECL}	PECL Input Voltage	V_{EE} = 0V	0 to + 6.0	V
V_{EE}	ECL Power Supply	V_{CC} = 0V	-6.0 to 0	V
V_{I_ECL}	ECL Input Supply	V_{CC} = 0V	-6.0 to 0	V
V_{I_DIFF}	Differential Input Voltage		0 to ± 1.6	V_{pp} [1]
I_{OUT}	Output Current	Continuous	50	mA
		Surge	100	
T_A	Operating Temperature Range	-	-40 to +85 [2]	°C
T_{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD_{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD_{MM}	Machine Model Electro Static Discharge	-	200	V
ESD_{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

[1] $V_{I\ DIFF}$ is the voltage difference between D and D^{-}

[2] For operation up to 105°C, contact Arizona Microtek

Table 10 - 10K ECL DC Characteristics

10K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1080	-890	-1020	-840	-980	-810	-910	-720	mV
V_{OL}	Output LOW Voltage[1]	-1950	-1650	-1950	-1630	-1950	-1630	-1950	-1595	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$	-1230	-430	-1170	-380	-1130	-360	-1060	-310	mV
	Input HIGH Voltage $\overline{EN}$	-1230	V_{CC}	-1170	V_{CC}	-1130	V_{CC}	-1060	V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$	-2300	-1500	-2260	-1480	-2240	-1480	-2190	-1445	mV
	Input LOW Voltage $\overline{EN}$	V_{EE}	-1500	V_{EE}	-1480	V_{EE}	-1480	V_{EE}	-1445	mV
V_{BB}	Reference Voltage	-1430	-1300	-1380	-1260	-1360	-1240	-1310	-1190	mV
I_{IH}	Input HIGH Current D/$\overline{D}$		60		60		60		60	µA
	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current	0.5		0.5		0.5		0.5		µA
I_{EE}	Power Supply Current		40		40		40		40	mA

[1] Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

Table 11 - 10K LVPECL DC Characteristics

10K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2220	2410	2280	2460	2320	2490	2390	2580	mV
V_{OL}	Output LOW Voltage[1,2]	1350	1650	1350	1670	1350	1670	1350	1705	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$[1]	2070	2870	2130	2920	2170	2940	2240	2990	mV
	Input HIGH Voltage $\overline{EN}$	2070	V_{CC}	2130	V_{CC}	2170	V_{CC}	2240	V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$[1]	1000	1800	1040	1820	1060	1820	1110	1855	mV
	Input LOW Voltage $\overline{EN}$	V_{EE}	1800	V_{EE}	1820	V_{EE}	1820	V_{EE}	1825	mV
V_{BB}	Reference Voltage[1]	1870	2000	1920	2040	1940	2060	1990	2110	mV
I_{IH}	Input HIGH Current D/$\overline{D}$		60		60		60		60	µA
	Input HIGH Current $\overline{EN}$		150		150		150		150	µA
I_{IL}	Input LOW Current D/$\overline{D}$	0.5		0.5		0.5		0.5		µA
	Input LOW Current $\overline{EN}$[3]	-300		-300		-300		-300		µA
I_{EE}	Power Supply Current		40		40		40		46	mA

1 For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.

2 Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

3 Specified with forced to V_{EE}.

Table 12 - 10K PECL DC Characteristics

10K PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3920	4110	3980	4160	4020	4190	4090	4280	mV
V_{OL}	Output LOW Voltage[1,2]	3050	3350	3050	3370	3050	3370	3050	3405	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$[1]	3770	4570	3830	4620	3870	4640	3940	4690	mV
	Input HIGH Voltage $\overline{EN}$	3770	V_{CC}	3830	V_{CC}	3870	V_{CC}	3940	V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$[1]	2700	3500	2740	3520	2760	3520	2810	3555	mV
	Input LOW Voltage $\overline{EN}$	V_{EE}	3500	V_{EE}	3520	V_{EE}	3520	V_{EE}	3555	mV
V_{BB}	Reference Voltage[1]	3570	3700	3620	3740	3640	3760	3690	3810	mV
I_{IH}	Input HIGH Current D/$\overline{D}$		60		60		60		60	µA
	Input HIGH Current $\overline{EN}$		150		150		150		150	µA
I_{IL}	Input LOW Current D/$\overline{D}$	0.5		0.5		0.5		0.5		µA
	Input LOW Current $\overline{EN}$[3]	-1400		-1400		-1400		-1400		µA
I_{EE}	Power Supply Current		40		40		40		40	mA

1 For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.

2 Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

3 Specified with forced to V_{EE}.

Table 13 - 100K ECL DC Characteristics

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V_{OL}	Output LOW Voltage[1]	-1900	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$	-1165	-390	-1165	-390	-1165	-390	-1165	-390	mV
	Input HIGH Voltage $\overline{EN}$	-1165	V_{CC}	-1165	V_{CC}	-1165	V_{CC}	-1165	V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$	-2250	-1475	-2250	-1475	-2250	-1475	-2250	-1475	mV
	Input LOW Voltage $\overline{EN}$	V_{EE}	-1475	V_{EE}	-1475	V_{EE}	-1475	V_{EE}	-1475	mV
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I_{IH}	Input HIGH Current D/$\overline{D}$		60		60		60		60	µA
	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current	0.5		0.5		0.5		0.5		µA
I_{EE}	Power Supply Current		40		40		40		46	mA

1 Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

Table 14 - 100K LVECL DC Characteristics

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2215	2420	2275	2420	2275	2420	2275	2420	mV
V_{OL}	Output LOW Voltage[1,2]	1400	1745	1400	1680	1400	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$[1]	2135	2910	2135	2910	2135	2910	2135	2910	mV
	Input HIGH Voltage $\overline{EN}$	2135	V_{CC}	2135	V_{CC}	2135	V_{CC}	2135	V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$[1]	1050	1825	1050	1825	1050	1825	1050	1825	mV
	Input LOW Voltage $\overline{EN}$	V_{EE}	1825	V_{EE}	1825	V_{EE}	1825	V_{EE}	1825	mV
V_{BB}	Reference Voltage[1]	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IH}	Input HIGH Current D/$\overline{D}$		60		60		60		60	µA
	Input HIGH Current $\overline{EN}$		150		150		150		150	µA
I_{IL}	Input LOW Current D/$\overline{D}$	0.5		0.5		0.5		0.5		µA
	Input LOW Current $\overline{EN}$[3]	-300		-300		-300		-300		µA
I_{EE}	Power Supply Current		40		40		40		46	mA

1 For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.

2 Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

3 Specified with forced to V_{EE}.

Table 15 – 100K PECL DC Characteristics

100K PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3915	4120	3975	4120	3975	4120	3975	4120	mV
V_{OL}	Output LOW Voltage[1,2]	3100	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$[1]	3835	4610	3835	4610	3835	4610	3835	4610	mV
	Input HIGH Voltage $\overline{EN}$	3835	V_{CC}	3835	V_{CC}	3835	V_{CC}	3835	V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$[1]	2750	3525	2750	3525	2750	3525	2750	3525	mV
	Input LOW Voltage $\overline{EN}$	V_{EE}	3525	V_{EE}	3525	V_{EE}	3525	V_{EE}	3525	mV
V_{BB}	Reference Voltage[1]	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current D/$\overline{D}$		60		60		60		60	µA
	Input HIGH Current $\overline{EN}$		150		150		150		150	µA
I_{IL}	Input LOW Current D/$\overline{D}$	0.5		0.5		0.5		0.5		µA
	Input LOW Current $\overline{EN}$[3]	-1400		-1400		-1400		-1400		µA
I_{EE}	Power Supply Current		40		40		40		46	mA

1 For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.

2 Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

3 Specified with forced to V_{EE}.

Table 16 - AC Characteristics

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC}=GND or V_{EE}=GND; V_{CC} = +3.0V to +5.5V)

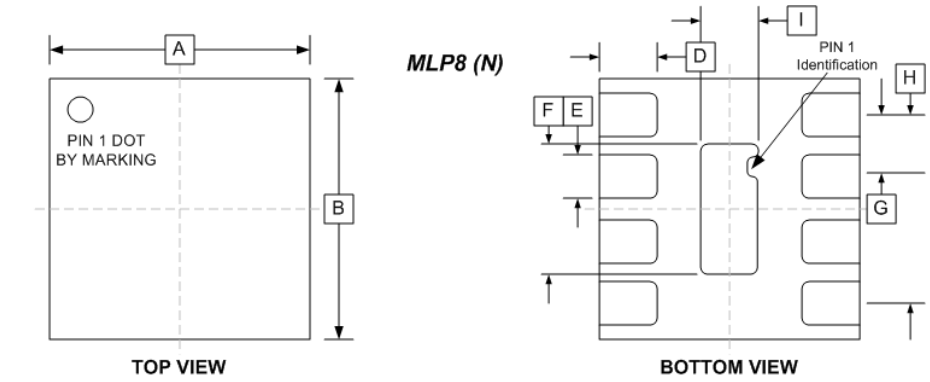
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}/t_{PHL}	Propagation Delay													
	D to Q/$\overline{Q}$	100		300	100		300	100	200	300	100		300	ps
	D to $Q_{HG}/\overline{Q}_{HG}$	150		450	150		450	150	290	450	150		450	ps
t_{SKEW}	Duty Cycle Skew[1]		5	20		5	20		5	20		5	20	ps
Vpp (AC)	Input Swing[2]	80		1000	80		1000	80		1000	80		1000	mV
t_r/t_f	Output Rise/Fall (20% - 80%)	80		240	80		240	80	135	240	80		240	ps

1 Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

2 V_{PP} is the peak-to-peak differential input swing for which AC parameters are guaranteed. The device has a voltage gain of ≈20 to Q/$\overline{Q}$ outputs and a voltage gain of ≈100 to $Q_{HG}/\overline{Q}_{HG}$ outputs.

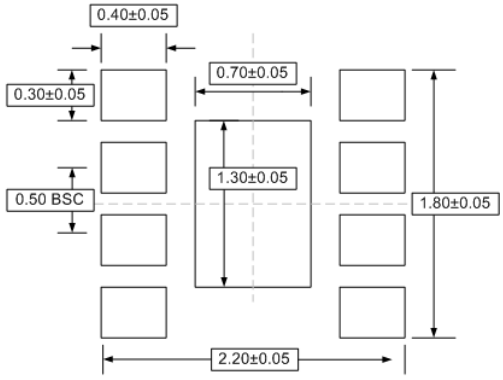
PACKAGE DIAGRAM

MLP8
Green/RoHS compliant/Pb-Free
MSL=1



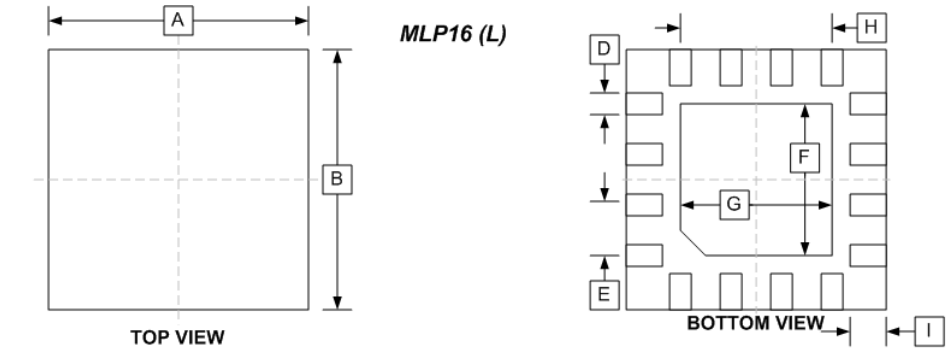
	MILLIMETERS	
DIM	MIN	MAX
A	2.00±0.050	
B	2.00±0.050	
C	0.75±0.050	
C_1	0.00	0.05
C_2	0.203 Ref.	
D	0.35±0.050	
E	0.25±0.050	
F	1.20±0.050	
G	0.500 BSC	
H	1.500 REF	
I	0.60±0.050	

PCB LAND PATTERN/FOOTPRINT

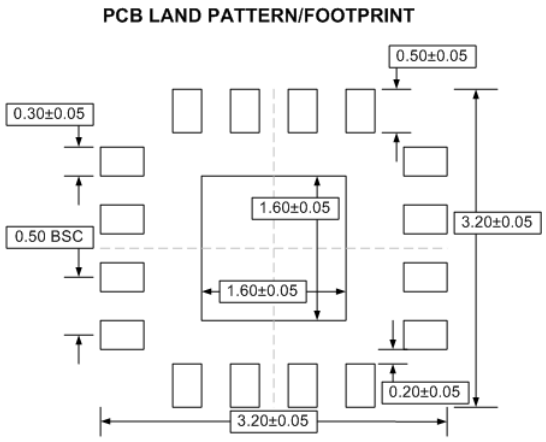


PACKAGE DIAGRAM

MLP16
Green/RoHS compliant/Pb-Free
MSL=1

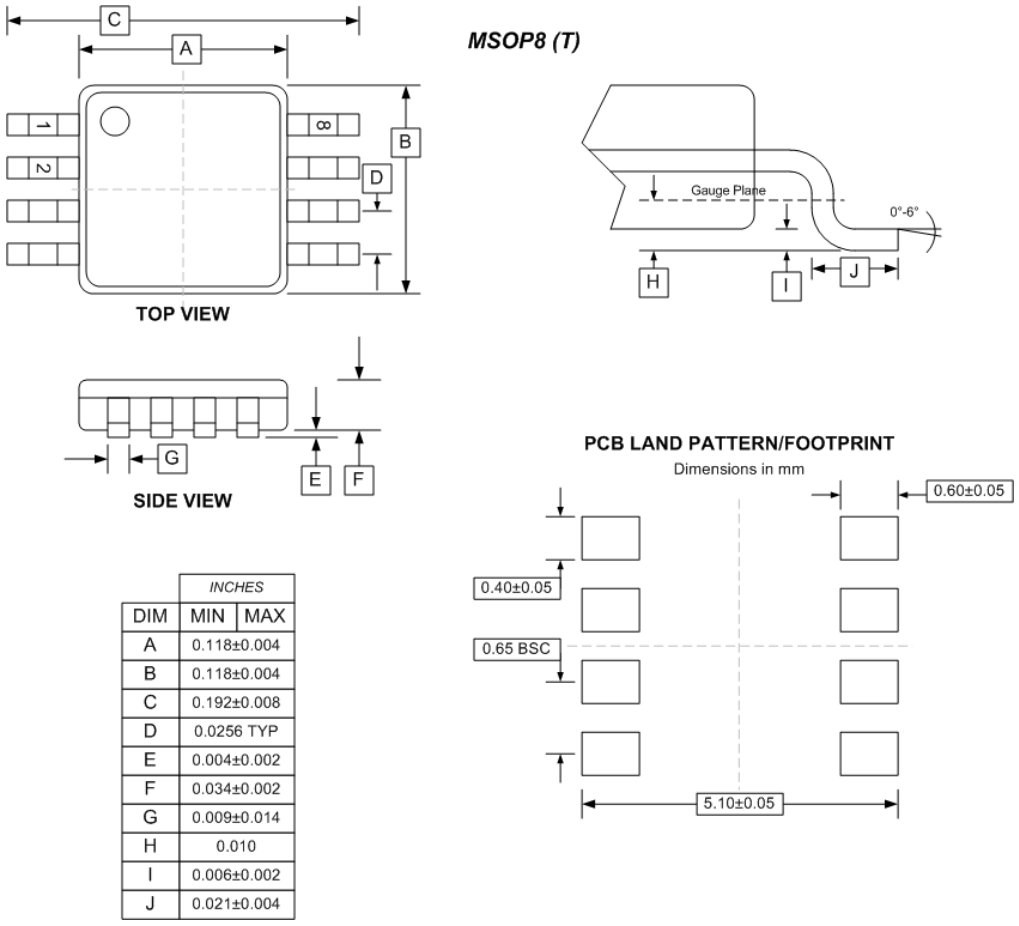


	MILLIMETERS	
DIM	MIN	MAX
A	3.00±0.050	
B	3.00±0.050	
C	0.85±0.050	
C_1	0.00	0.05
C_2	0.203 REF	
D	0.23±0.050	
E	0.50 BSC	
F	1.55±0.050	
G	1.55±0.050	
H	1.500 Ref	
I	0.40±0.050	



PACKAGE DIAGRAM

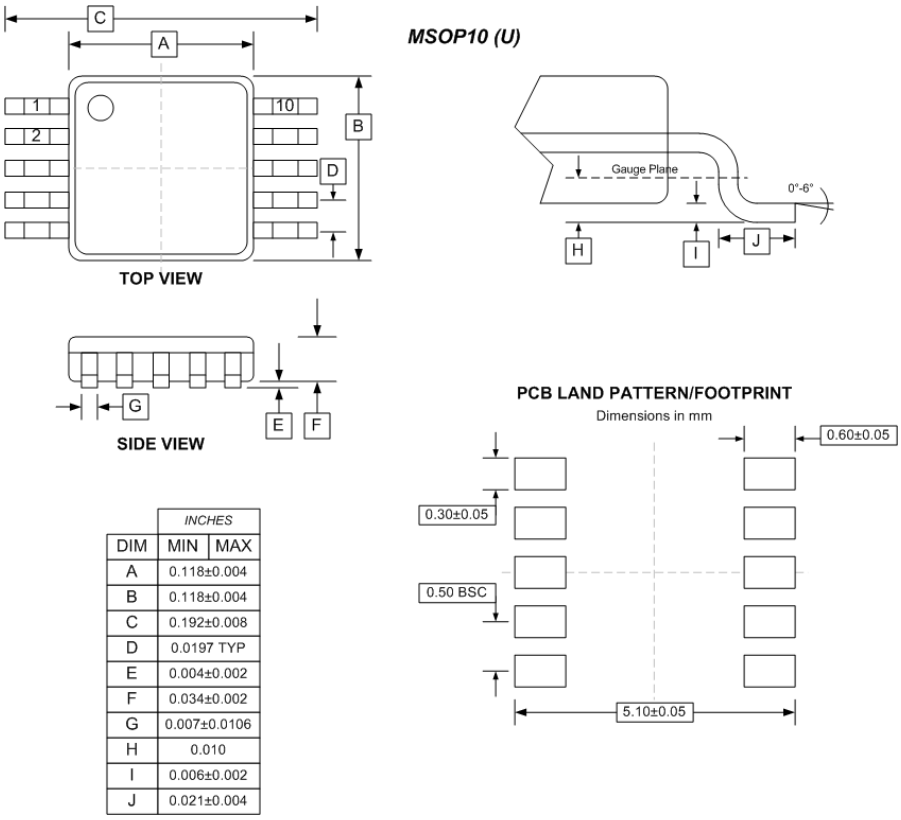
MSOP8
Green/RoHS compliant/Pb-Free
MSL=1



	INCHES	
DIM	MIN	MAX
A	0.118±0.004	
B	0.118±0.004	
C	0.192±0.008	
D	0.0256 TYP	
E	0.004±0.002	
F	0.034±0.002	
G	0.009±0.014	
H	0.010	
I	0.006±0.002	
J	0.021±0.004	

PACKAGE DIAGRAM

MSOP10
Green/RoHS compliant/Pb-Free
MSL=1



	INCHES	
DIM	MIN	MAX
A	0.118±0.004	
B	0.118±0.004	
C	0.192±0.008	
D	0.0197 TYP	
E	0.004±0.002	
F	0.034±0.002	
G	0.007±0.0106	
H	0.010	
I	0.006±0.002	
J	0.021±0.004	