AZP52

Low Phase Noise Sine Wave / CMOS to LVPECL Buffer / Translator

www.azmicrotek.com

DESCRIPTION

The AZP52 is a sine wave/CMOS to LVPECL buffer/translator optimized for very low phase noise (-165dBc/Hz). It is particularly useful in converting crystal or SAW based oscillators into LVPECL outputs greater than 800MHz of bandwidth. For greater bandwidth, refer to the AZP63.

The AZP52 is one of a family of parts that provide options of fixed ÷1, fixed ÷2 and selectable ÷1, ÷2 modes as well as active high enable or active low enable to oscillator designers. Refer to Table 2 for the comparison of parts within the AZP5x and AZP63 family.

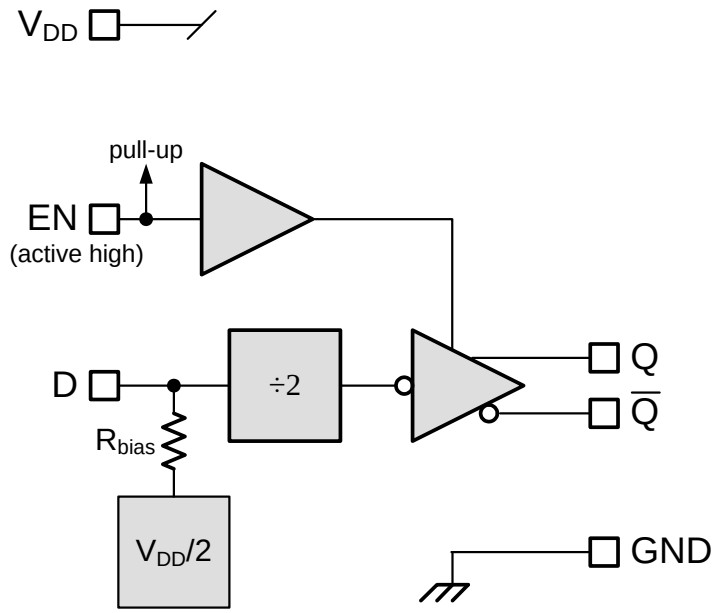
FEATURES

- LVPECL outputs optimized for very low phase noise (-165dBc/Hz)
- Greater than 800MHz bandwidth
- Fixed ÷2 output
- 3.0V to 3.6V operation

APPLICATIONS

- PECL clock sources
- Crystal or SAW based oscillators with LVPECL output

BLOCK DIAGRAM



PACKAGE AVAILABILITY

- SC70-6
  - Green/RoHS Compliant/Pb-Free

Order Number	Package	Marking
AZP52SG[1]	SC70-6	C <Date Code>[2]

[1] Tape & Reel - Add 'R1' at end of order number for 7in (1k parts), 'R2' (2.5k) for 13in

[2] See www.azmicrotek.com for date code format

PIN DESCRIPTION AND CONFIGURATION

Table 1 - Pin Description

Pin	Name	Type	Function
1	V_{DD}	Power	Positive Supply
2	GND	Power	Negative Supply
3	D	Input	Sine or CMOS Input
4	EN	Input	Enable
5	$\overline{Q}$	Output	LVPECL Output
6	Q	Output	LVPECL Output

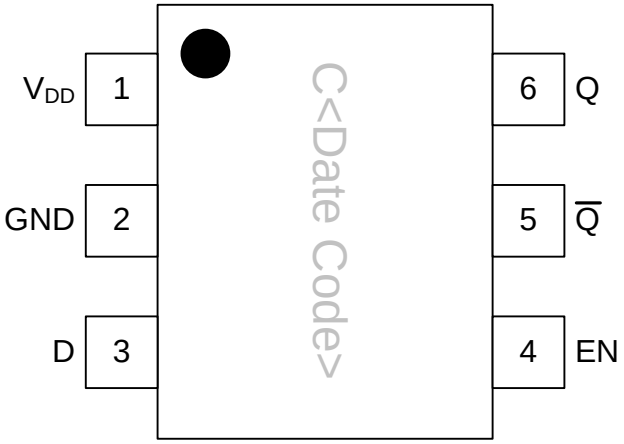


Figure 1 – Pin Configuration

ENGINEERING NOTES

FUNCTIONALITY

The AZP52 is one of a family of parts that provide options of fixed ÷1, fixed ÷2 and selectable ÷1, ÷2 modes as well as active high enable or active low enable to oscillator designers. Table 2 details the differences between the parts to assist designers in selecting the optimal part for their design.

Table 3 lists the specific AZP52 functional operation.

Figure 2 plots the S-parameters of the D input. S-parameter and IBIS model files for the AZP52 are also available for download.

Table 2 - AZP51-54 & AZP63 Family

Part Number	Divide Ratio	EN Logic	EN pull-up/pull-down	Bandwidth
AZP51	÷1	active HIGH	Pull-up	> 800MHz
AZP52	÷2	active HIGH	Pull-up	> 800MHz
AZP53	Selectable ÷1 or ÷2	selectable	selectable	> 800MHz
AZP54	÷1	active LOW	Pull-down	> 800MHz
AZP63	Selectable ÷1 or ÷2	selectable	selectable	≥ 1GHz

Table 3 - AZP52 Functional Operation

	Inputs		Outputs	
Part Number	**EN**	**D**	**Q**	**$\bar{Q}$**
AZP52	High, NC[1]	Low	Low[4]	High[4]
		High	High[4]	Low[4]
	Low	X[2]	Z[3]	Z[3]

[1] Not connected

[2] Don't care

[3] Tri-State

[4] Every other clock cycle

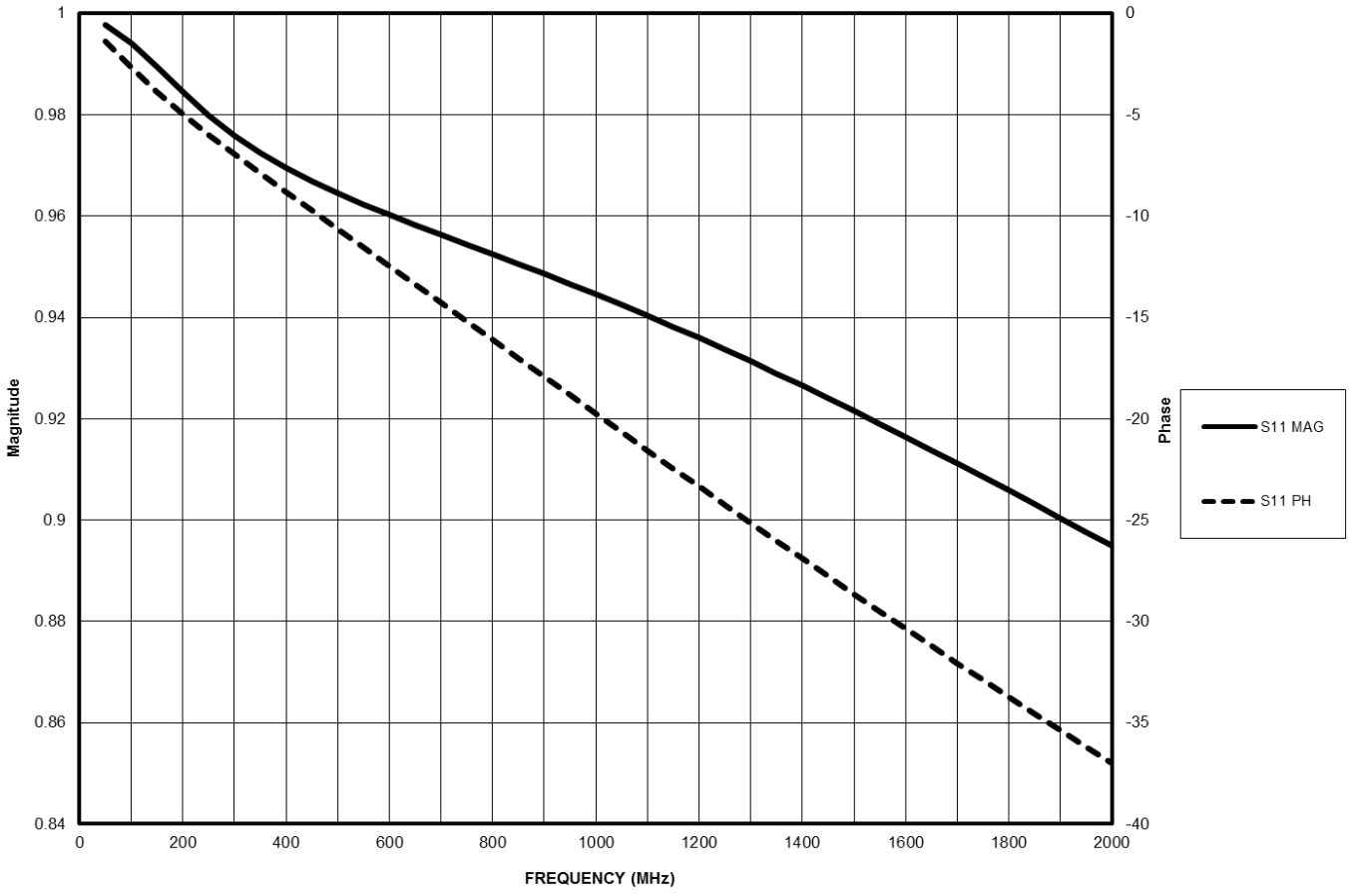


Figure 2- S11, Parameters, D Input

INPUT TERMINATION

The D input bias is $V_{DD}/2$ fed through an internal 10kΩ resistor. For clock applications, an input signal of at least $750mV_{pp}$ ensures the AZP52 meets AC specifications. The input should also be AC coupled to maintain a 50% duty cycle on the outputs. The input can be driven to any voltage between 0V and V_{DD} without damage or waveform degradation.

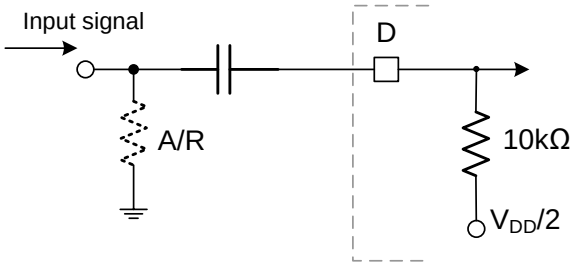


Figure 3 - Input Termination

OUTPUT TERMINATION TECHNIQUES

The LVPECL compatible output stage of the AZP52 uses a current drive topology to maximize switching speed as illustrated below in Figure 4. Two current source PMOS transistors (M1-M2) feed the output pins. M5 is an NMOS current source which is switched by M3 and M4. When M4 is on, M5 takes current from M2. This produces an output current of 5.1mA (low output state). M3 is off, and the entire 21.1mA flows through the output pin. The associated output voltage swings match LVPECL levels when external 50Ω resistors terminate the outputs.

Both Q and $\overline{Q}$ should always be terminated identically to avoid waveform distortion and circulating current caused by unsymmetrical loads. This rule should be followed even if only one output is in use.

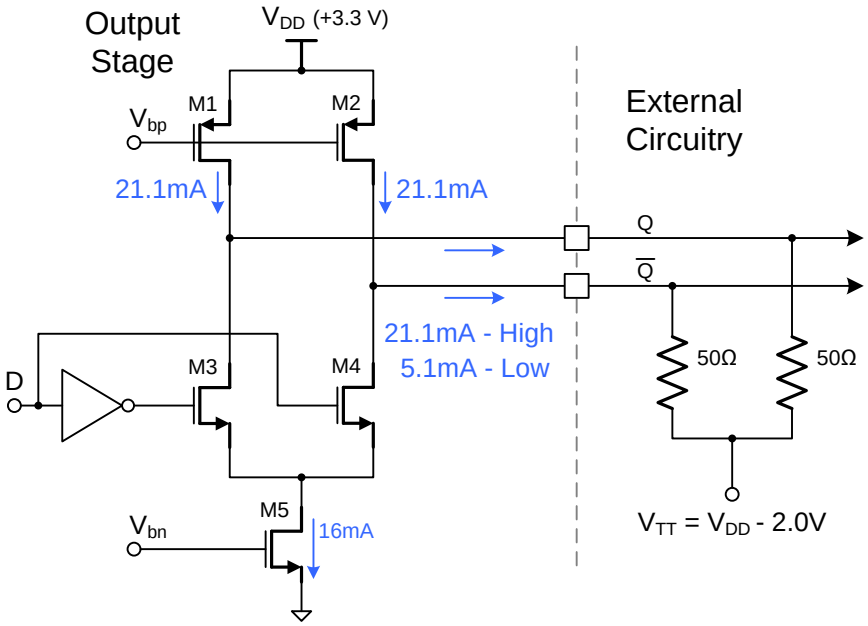


Figure 4 - Typical Output Termination

DUAL SUPPLY LVPECL OUTPUT TERMINATION

The standard LVPECL loads are a pair of 50Ω resistors connected between the outputs and V_{DD}-2.0V (Figure 4). The resistors provide both the DC and the AC loads, assuming 50Ω interconnect. If an additional supply is available within the application, a four resistor termination configuration is possible (Figure 5).

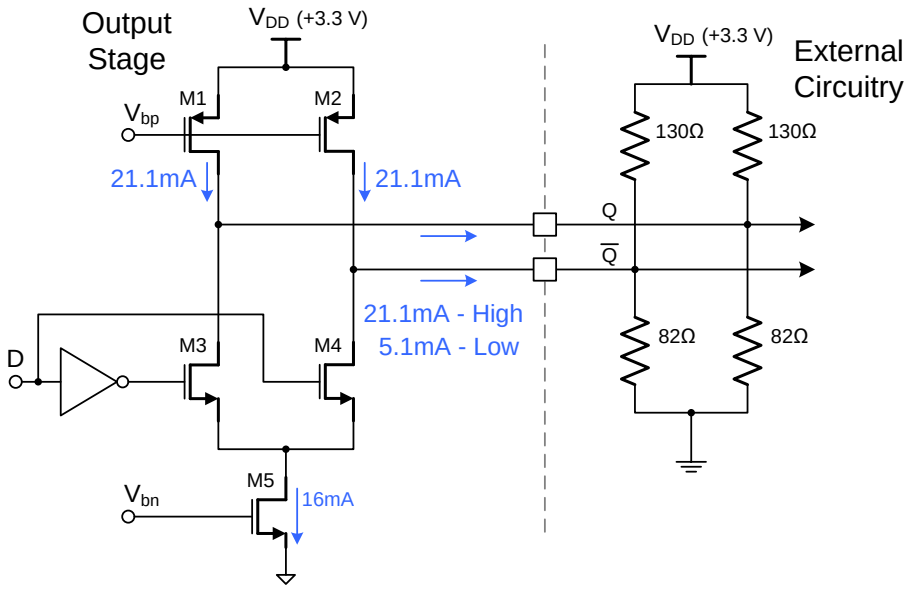


Figure 5 - Dual Supply Output Termination

THREE RESISTOR TERMINATION

Another termination variant eliminates the need for the additional supply (Figure 6). Alternately three resistors and one capacitor accomplish the same termination and reduce power consumption.

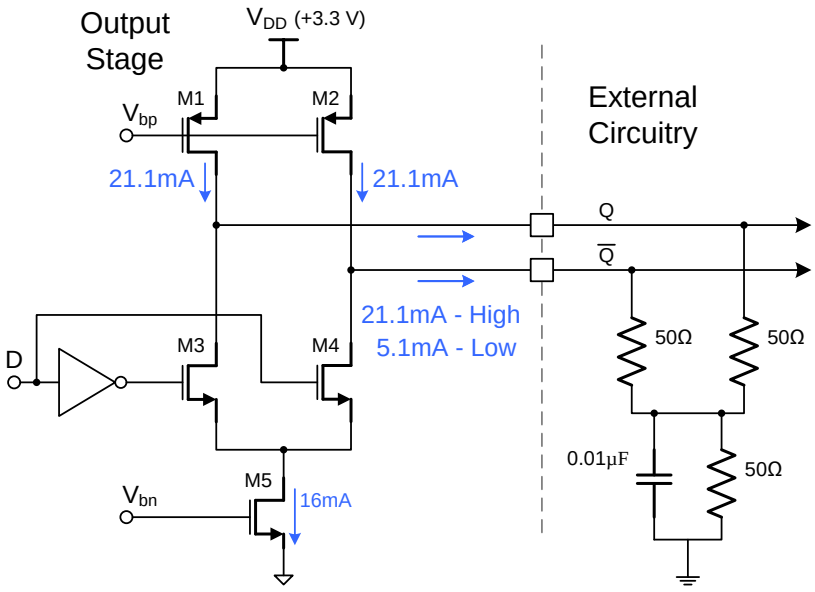


Figure 6 - Three Resistor Termination

EVALUATION BOARD (EBP53)

Arizona Microtek's evaluation board EBP53 provides the most convenient way to test and prototype AZP52 series circuits. Built for the AZP53Q 1.5x1.0 mm package, it is designed to support both dual and single supply operation. Dual supply operation (V_{DD}=+2.0V, V_{SS}=-1.3V) enables direct coupling to 50Ω time domain test equipment (Figure 7).

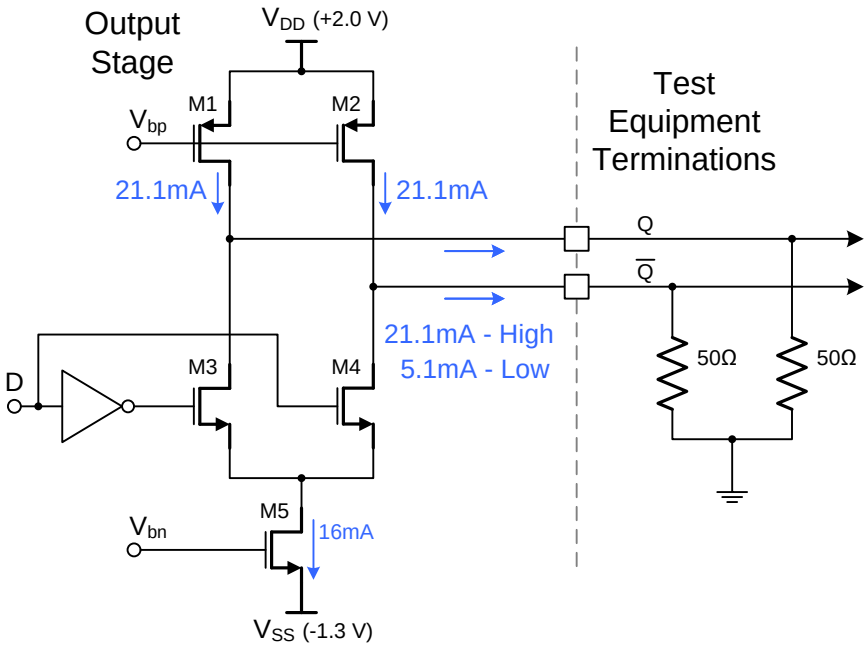


Figure 7 - Split Supply LVPECL Output Termination

AC TERMINATION

Clock applications or phase noise/frequency domain testing scenarios typically require AC coupling. Figure 8 below shows the AC coupling technique. The 200Ω resistors form the required DC loads, and the 50Ω resistors provide the AC termination. The parallel combination of the 200Ω and 50Ω resistors results in a net 40Ω AC load termination. In many cases this will work well. If necessary, the 50Ω resistors can be increased to about 56Ω. Alternately, bias tees combined with current setting resistors will eliminate the lowered AC load impedance. The 50Ω resistors are typically connected to ground but can be connected to the bias level needed by the succeeding stage.

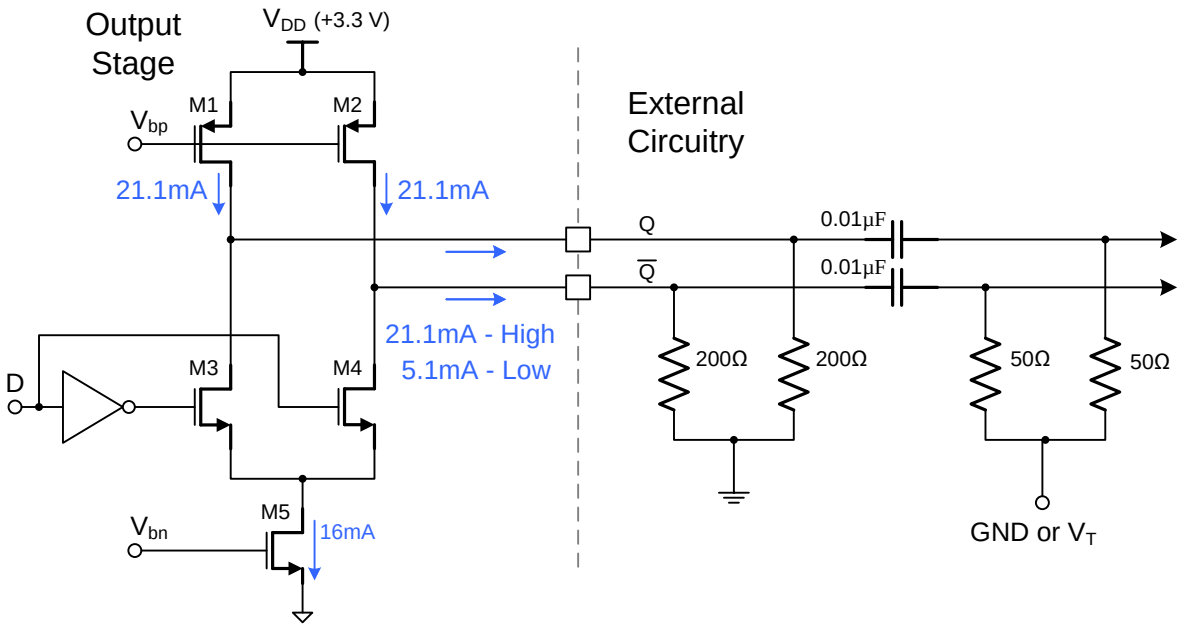


Figure 8 - AC Termination

PERFORMANCE DATA

Table 4 - Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{DD}	Power Supply	0 to +5.5	V
V_I	Input Voltage	-0.5 to V_{DD} + 0.5	V
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
ESD_{HBM}	Human Body Model	2500	V
ESD_{MM}	Machine Model	200	V
ESD_{CDM}	Charged Device Model	2500	V

Table 5 - DC Characteristics

DC Characteristics (V_{DD} = 3.0V to 3.6V unless otherwise specified, T_A = -40 to 85 °C)

Symbol	Characteristic	Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage[1]	-40 C	V_{DD} = 3.3V	2.05		2.415	V
		25 C		2.05		2.48	
		85 C		2.05		2.54	
V_{OL}	Output LOW Voltage[1]	-40 C	V_{DD} = 3.3V	1.365		1.615	V
		25 C		1.43		1.68	
		85 C		1.49		1.74	
I_Z	Output Leakage Current, Tri-state[2]	EN=Low		-10		10	µA
V_{IH}	High Level Input Voltage	EN		2			V
V_{IL}	Low Level Input Voltage	EN				0.8	V
I_{PD}	Pull-down Current	EN			-2.2		µA
R_{BIAS}	Bias Resistor	D Input to Internal $V_{DD}/2$ Reference			10k		Ω
I_{DD}	Power Supply Current				22	35	mA
I_{DDZ}	Power Supply Current	D Input ≤ V_{IL}				8	mA
	Outputs Tri-state[1]	EN=Low					

[1] Specified with outputs terminated through 50Ω resistors to V_{DD} - 2V or Thevenin equivalent.

[2] Measured at Q / $\overline{Q}$ pins.

Table 6 - AC Characteristics

AC Characteristics (V_{DD} = 3.0V to 3.6V, T_A = -40 to 85 °C)

AC Specifications guaranteed by design

Symbol	Characteristic	Min	Typ	Max	Unit
t_r / t_f	Output Rise/Fall[1,2] (20% - 80%)	80		250	ps
f_{MAX}	Maximum Input Frequency - Sine wave[2]			1300	MHz
V_{INMAX}	Maximum Recommended Input Signal			V_{DD}	Vpp
V_{INMIN}	Minimum Recommended Input Signal	0.2			Vpp
t_{PLH}	Propagation Delay	938		1614	ps
t_{PHL}	Propagation Delay	938		1614	ps
j_{RMS}	RMS Jitter: 12kHz - 20MHz, 155MHz Center Freq		36		fs
n_P	Phase Noise[1,2] - 1MHz offset		-165		dBc/Hz

[1] Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V or Thevenin equivalent.

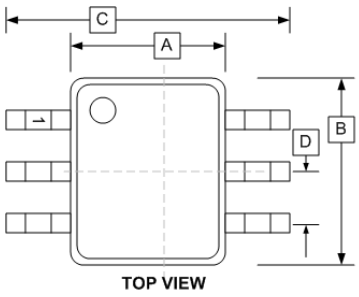
[2] 1.5 v p-p sine wave input, AC coupled to D pin.

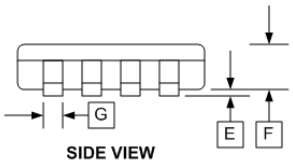
PACKAGE DIAGRAM

SC70-6

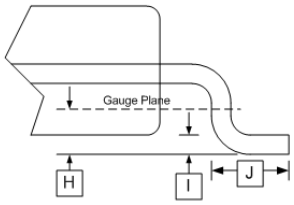
Green/RoHS compliant/Pb-Free

MSL=1





SC70-6 (S)



DIM	MILLIMETERS MIN	MAX
A	1.15	1.35
B	1.85	2.25
C	2.00	2.30
D	0.65 BSC	
E	0.00	0.09
F	0.80	0.91
G	0.15	0.30
H	2.467	
I	0.08	0.25
J	0.21	0.41

PCB LAND PATTERN/FOOTPRINT

Dimensions in mm